



StarFive
赛昉科技

StarFive JH-7110 Product Brief

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Legal Statements

Important legal notice before reading this documentation.

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Preface

About this guide and technical support information.

About this document

This document mainly provides the users with the general information and feature description for StarFive next generation SoC platform - JH-7110.






Revision History

Table 0-1 Revision History

| Version | Released | Revision |
|---------|------------|--|
| 1.5 | 2024/08/29 | Updated Block Diagram (on page 8) . |
| 1.4 | 2023/08/02 | Synchronized the document with Datasheet. |
| 1.3 | 2022/12/8 | Added GMAC limitations. |
| 1.2 | 2022/10/20 | Refined block diagram and refined MIPI output specs. |
| 1.1 | 2022/09/15 | Updated block diagram in sync with Datasheet. |
| 1.0 | 2022/08/23 | 1st official release of the document. |

Notes and notices

The following notes and notices might appear in this guide:

-  **Tip:**
Suggests how to apply the information in a topic or step.
-  **Note:**
Explains a special case or expands on an important point.
-  **Important:**
Points out critical information concerning a topic or step.
-  **CAUTION:**
Indicates that an action or step can cause loss of data, security problems, or performance issues.
-  **Warning:**
Indicates that an action or step can result in physical harm or cause damage to hardware.

Contents

List of Tables.....5

List of Figures.....6

Legal Statements.....2

Preface.....3

1. Introduction.....7

2. Block Diagram.....8

3. Application.....9

4. Highlighted Feature.....10

5. Feature.....11

List of Tables

| | |
|---------------------------------|---|
| Table 0-1 Revision History..... | 3 |
|---------------------------------|---|



List of Figures

| | |
|-------------------------------|---|
| Figure 2-1 Block Diagram..... | 8 |
|-------------------------------|---|



1. Introduction

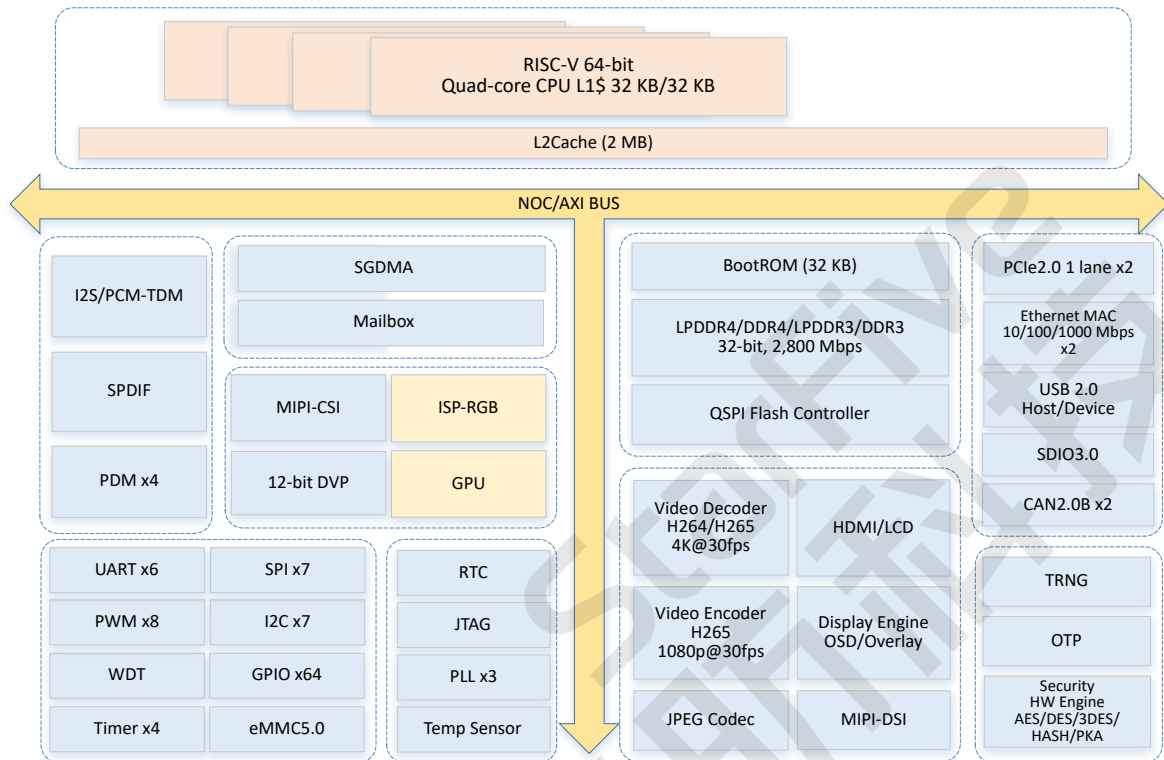
JH-7110 is a high-performance RISC-V SoC for featuring high-performance, low-power-consumption, rich interface options, and powerful image and video processing capabilities.

JH-7110 is equipped with a 64-bit high-performance quad-core RISC-V processor core sharing 2 MB of cache coherency, whose working frequency is 1.5 GHz. JH-7110 has a rich high-speed native interface, supports the Linux operating system, and has powerful image and video processing system. The StarFive ISP is compatible with mainstream camera sensors, built-in image/video processing subsystem supports H.264/H.265/JPEG codec. The integrated GPU makes its image processing capabilities stronger, such as 3D rendering. With high-performance, OpenCL/OpenGL ES/Vulkan support, JH-7110 can further enhance intelligence and efficiency. JH-7110 can complete a variety of complex image/video processing and intelligent visual calculations. Also, it meets multiple visual real-time processing requirements at the edge.

2. Block Diagram

The following figure shows the block diagram of JH-7110.

Figure 2-1 Block Diagram



Note:

- JH-7110 supports one USB port. One of the PCIe2.0 lanes can be shared by USB3.0.
- JH-7110 supports one port for SDIO and one port for eMMC, or both ports for SDIO.

3. Application

An introduction to the application scenarios.

JH-7110 applies to the following scenarios.

- Commercial Electronics
 - Personal *Single Board Computer (SBC)*
 - Home NAS
 - Router (Soft routing)
 - Notebook computer
- Smart Home
 - Sweeping robot
 - Intelligent home appliances
 - Video surveillance
- Industrial Intelligence
 - Industrial robot
 - Unmanned store

4. Highlighted Feature

JH-7110 has the following highlighted features.

- RISC-V U74 quad-core with 2 MB L2 cache
- Support Linux OS with kernel versions 5.10 and 5.15
- CPU work frequency up to 1.5 GHz
- GPU IMG BXE-4-32
- 32-bit LPDDR4/DDR4/LPDDR3/DDR3, up to 2,800 Mbps
- Video decoder supports up to 4K@30fps and multi-stream for H.264/H.265
- Video encoder supports up to 1080p@30fps and multi-stream for H.265
- Provide JPEG encoder/decoder
- Support up to 1080p@30fps full-functional ISP
- Support video input: 1 × DVP and 1 × MIPI-CSI with 4D1C up to 4K@30fps
- Support video output: MIPI display output with 4D1C up to 1080p@60fps
- Support 1 × HDMI2.0 port display up to 4K@30fps
- Support 24-bit RGB parallel interface up to 1080p@30fps
- Support 2 × PCIe2.0, 1 lane
- Support USB3.0 Host/Device (By reusing 1 of the PCIe2.0 lanes)
- Support 2 × Ethernet MAC 1,000 Mbps, 2 × CAN2.0B
- Support IEEE 1588-2002 and IEEE 1588-2008 standards
- Support TRNG and support OTP, DMA, QSPI, and other peripherals
- Dedicated audio processing and sub-system

5. Feature

CPU Subsystem

- 64-bit high-performance RISC-V CPU quad-core
 - Support RV64GC RISC-V ISA
 - L1-cache: I\$32 KB/D\$32 KB
 - Cache coherence for quad-core
- 32-bit RISC-V CPU core
 - Support RV32IMFC RISC-V ISA
 - 16 KB I-cache only
- L2-cache up to 2 MB cache size
- Dual DMA controllers support up to 16+4 channels

Memory and Storage

- BUS RAM up to 256 KB
- DDR controller support 1 channel of x32
 - DDR4/3 and LPDDR4/3 for 2800 Mbps
 - Support 2 pieces of x16 or 1pcs of x32 devices
 - Support DDR memory density up to 8 GB
- QSPI controller support external flash memory
 - Support XIP mode and Page mode
 - Separate 1/2/4 data width
 - Support SPI Nor Flash size up to 16 MB
 - Support SPI Nand Flash size up to 2 GB

GPU Subsystem

- Support OpenCL 3.0
- Support OpenGL ES 3.2
- Support Vulkan 1.2

Video Processing Subsystem

- Camera MIPI Interface
 - MIPI CSI-2 RX DPHY
- Up to 6 lanes of 1.5 Gbps
- Support 4D1C × 1 MIPI sensors
- Support 2D1C × 1 MIPI sensors
- ISP (Image Signal Process)
 - Support 1 × MIPI CSI channel and 1 × DVP input channel
 - Support up to 1080p@30fps CMOS RGB image sensor
 - ISP core support

- Defective pixel correction
- R/G/B LUT, AE/AWB/AF
- Histogram analysis
- Lens Shading/Color Shading
- Sensor spatial crosstalk cancellation
- Global tone mapping/Spatial noise reduction
- Seamless digital scale down from 1/4x to 1x
- Video Encoder
 - H.265 Encoder, 1080p@30fps
 - Support I/P type slice
 - High-performance CABAC encoding
 - Support Region of Interest (ROI)
- Video Decoder
 - 4K@60fps or 1080p@30fps
 - Compatible with the ITU-T Recommendation H.264
 - Compatible with ISO/IEC 23008-2 H.265
 - Support Format 420, 8-bit/10-bit
 - Support I/P type slice
 - H.265 Main/Main10, L5.1
 - H.264 High/High10, L5.2
- JPEG
 - Up to 290 MPixel/Sec for YUV420, 210 MPixel/Sec for YUV422, 140 MPixel/Sec for YUV444
 - Bit rate 480 Mbps (MJPEG 8M@30fps 422 1:8)
 - Compliant with Baseline/Extended sequential ISO/IEC 10918-1 JPEG
 - Compliant with Motion JPEG
 - Support from 16x16 pixels to 32 K × 32 K (32,768 × 32,768)

Display Subsystem

- Display
 - Support 1 × HDMI 2.0 up to 4 K@30fps display
 - RGB656, RGB888 I/F, up to 1080p@30fps display
 - Support 6 image layers shared by 2 display panels (screens)
 - Support 1/64-64 times scaler (1/64 not covered)
 - Support MIPI TX DPHY lane connected with panel module
- MIPI Display Interface
 - MIPI TX DSI Controller for single display output
 - MIPI TX DPHY support up to 4D1C lanes
 - Data rate support up to 2.5 Gbps

Connectivity Subsystem

- 2x PCIe2.0 controller with integrated PHY
 - X1 PCI Express Core
 - Support link rate of 5 GT/s per lane
- USB 2.0 host/device mode with high speed and full speed
- 2 × Ethernet GMAC for 10/100/1000 Mbps with RGMII
- Ethernet GMAC supports data transfer rates of 10/100/1,000 Mbps auto-negotiation using the following PHY models
 - YT8521DH/DC
 - YT8531DH/DC
- Ethernet GMAC supports data transfer rates of 1,000 Mbps only using all other PHY models
- 2 × SDIO 3.0/eMMC 5.0 host controllers
- 2 × CAN2.0B data rates up to 5 Mbps

Security Subsystem

- Encrypt Engines: AES; DES/3DES; HASH; PKA
- Compliant with TRNG
- Support 256-bit random number generation
- 512 × 32-bit (2 KB) of OTP for key data on-die storage

Audio Interface

- 8 channel TX and RX I2S/PCM TDM
- Provide 4 sets of I2S/PCM I/F and support DMA interface
- Provide 2 sets of SPDIF and support RX mode and TX mode
- 4-channel PDM input for digital MIC application

Rich System Peripherals

- 6 × UART
- 7 × I2C
- 7 × SPI
- 2 × SDIO
- 1 × DPI (Parallel RGB Display)
- 1 × PCM/I2S
- 7 × 32-bit timers
- 1 × temperature sensor
- 2 × INTC
- 8 × PWM outputs
- 1 × 32-bit WDT reset output
- 64 × GPIO
- 1 × DVP sensor input interface
- 3 × GPCLK outputs

Package

- Body Size 17 × 17 mm, 0.65 mm ball pitch, FCBGA 625 balls

Power Supply

- 0.9 V core voltage
- 3.3 V/2.5 V/1.8 V I/O voltage

