StarFive 赛昉科技

StarFive JH-7110 Technical Reference Manual

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Legal Statements

Important legal notice before reading this documentation.

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Preface

About this guide and technical support information.

About this document

This document mainly provides the users with the technical reference information of the StarFive SoC JH-7110.

Revision History

Table 0-1 Revision History

Version	Released	Revision
Preliminary V2	2023/04/24	Refined the GPIO *(on page 82)* section per comments from the community users and added descriptions for ISP relevant registers.
Preliminary	2023/02/02	Preliminary release for customer preview. Please know the preliminary release is for preview only, any content inside can be updated without previous notice.

Notes and notices

The following notes and notices might appear in this guide:

- **Tip:**
  Suggests how to apply the information in a topic or step.
- **Note:**
  Explains a special case or expands on an important point.
- **Important:**
  Points out critical information concerning a topic or step.
- **CAUTION:**
  Indicates that an action or step can cause loss of data, security problems, or performance issues.
- **Warning:**
  Indicates that an action or step can result in physical harm or cause damage to hardware.

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1. System Overview

1.1. Introduction

JH-7110 is a high-performance RISC-V SoC featuring high-performance, low-power-consumption, rich interface options, and powerful image and video processing capabilities.

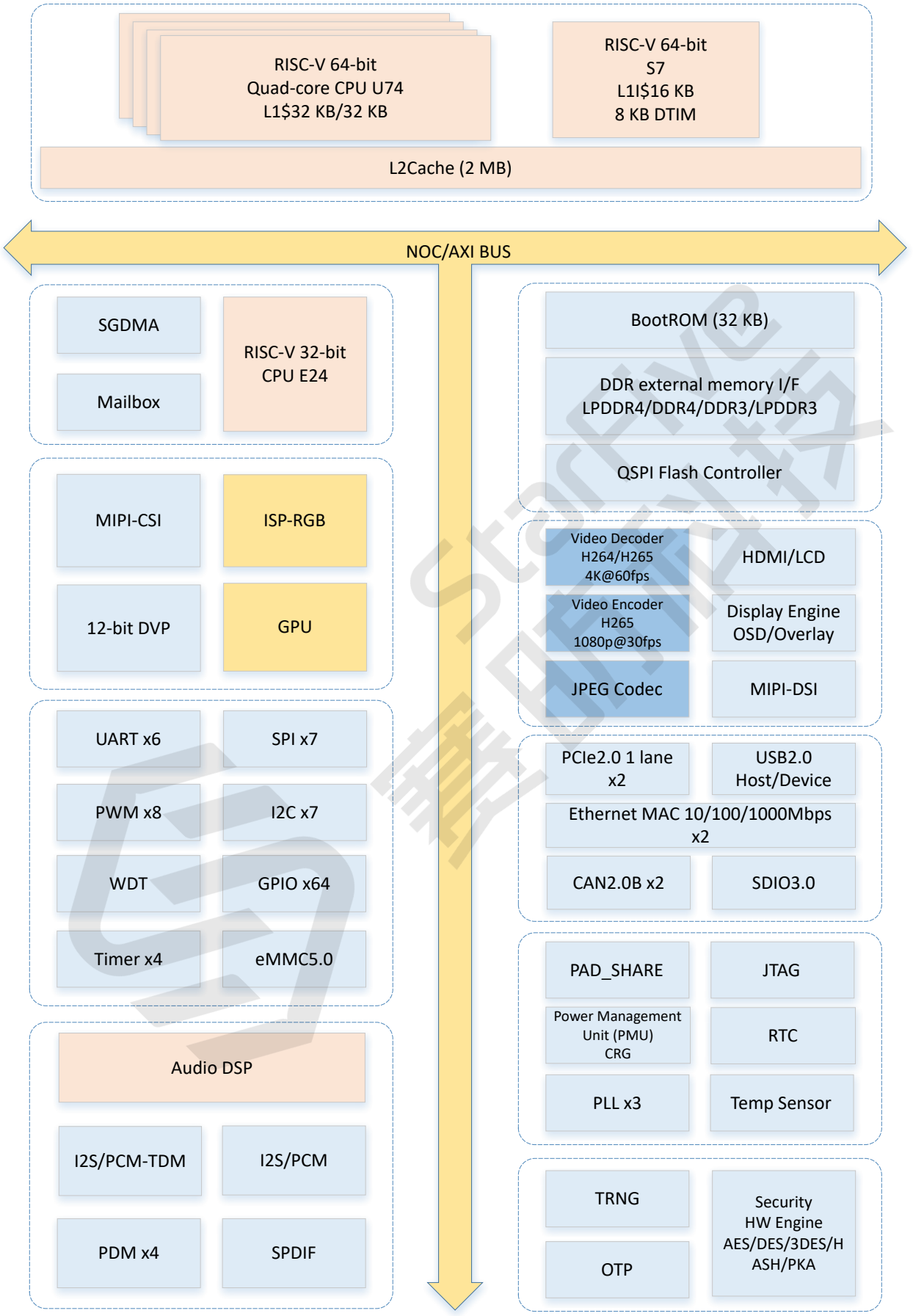
JH-7110 is equipped with a 64-bit high-performance quad-core RISC-V processor core sharing 2 MB of cache coherency, whose working frequency is 1.5 GHz. JH-7110 has a rich high-speed native interface, supports the Linux operating system, and has powerful image and video processing system. The StarFive ISP is compatible with mainstream camera sensors, built-in image/video processing subsystem supports H.264/H.265/JPEG codec. The integrated GPU makes its image processing capabilities stronger, such as 3D rendering. With high-performance, OpenCL/OpenGL ES/Vulkan support, JH-7110 can further enhance intelligence and efficiency. JH-7110 can complete a variety of complex image/video processing and intelligent visual calculations. Also, it meets multiple visual real-time processing requirements at the edge.

1.2. Block Diagram

The following figure shows the block diagram of JH-7110.

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Figure 1-1 Block Diagram



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Note:

- JH-7110 supports one USB port. One of the PCIe2.0 lanes can be shared by USB3.0.
- JH-7110 supports one port for SDIO and one port for eMMC, or both ports for SDIO.

1.3. Highlighted Feature

JH-7110 has the following highlighted features.

- RISC-V U74 quad-core and S7 monitor core with 2 MB L2 cache
- Support Linux OS with kernel versions 5.10 and 5.15
- CPU work frequency up to 1.5 GHz
- GPU IMG BXE-4-32
- 32-bit LPDDR4/DDR4/LPDDR3/DDR3, up to 2,800 Mbps
- Video decoder supports up to 4K@30fps and multi-stream for H.264/H.265
- Video encoder supports up to 1080p@30fps and multi-stream for H.265
- Provide JPEG encoder/decoder
- Support up to 1080p@30fps full-functional ISP
- Support video input: 1 × DVP and 1 × MIPI-CSI with 4D1C up to 4K@30fps
- Support video output: MIPI display output with 4D1C up to 1080p@60fps
- Support 1 × HDMI2.0 port display up to 4K@30fps
- Support 24-bit RGB parallel interface up to 1080p@30fps
- Support 2 × PCIe2.0, 1 lane
- Support USB3.0 Host/Device (By reusing 1 of the PCIe2.0 lanes)
- Support 2 × Ethernet MAC 1,000 Mbps, 2 × CAN2.0B
- Support IEEE 1588-2002 and IEEE 1588-2008 standards
- Support TRNG and support OTP, DMA, QSPI, and other peripherals
- Dedicated audio processing and sub-system

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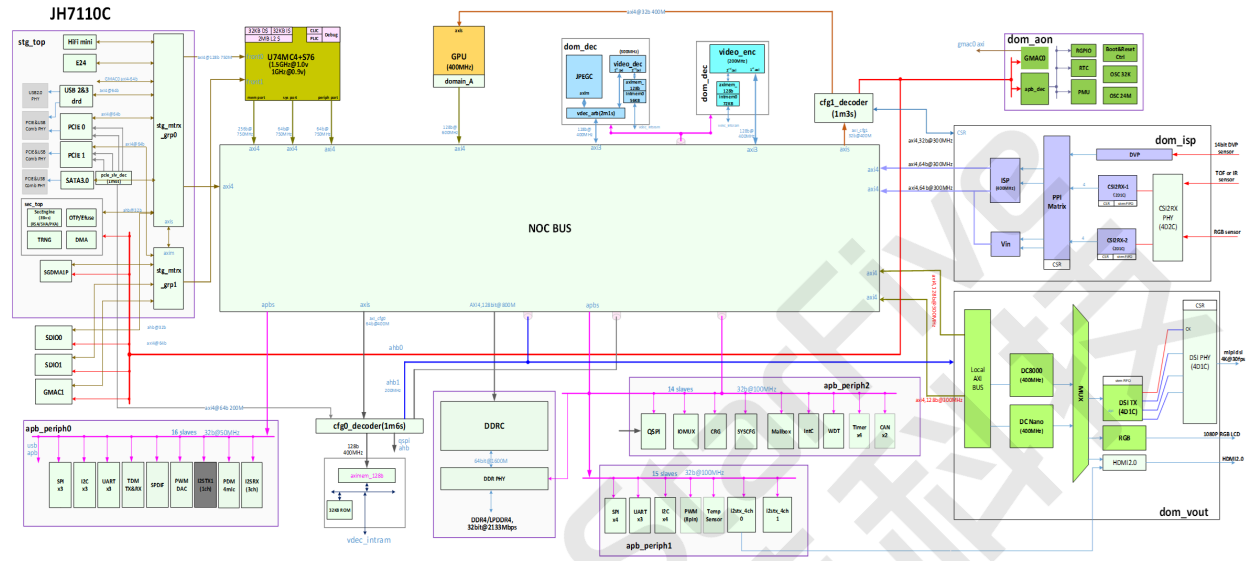
2. System Architecture

JH-7110 provides 2 processor cores, U74MC and E24.

They communicate with each other through mailbox.

The system block diagram of JH-7110 is shown in the following figure.

Figure 2-1 System Architecture



2.1. Bus Connection

The system bus connection is shown in the following table.

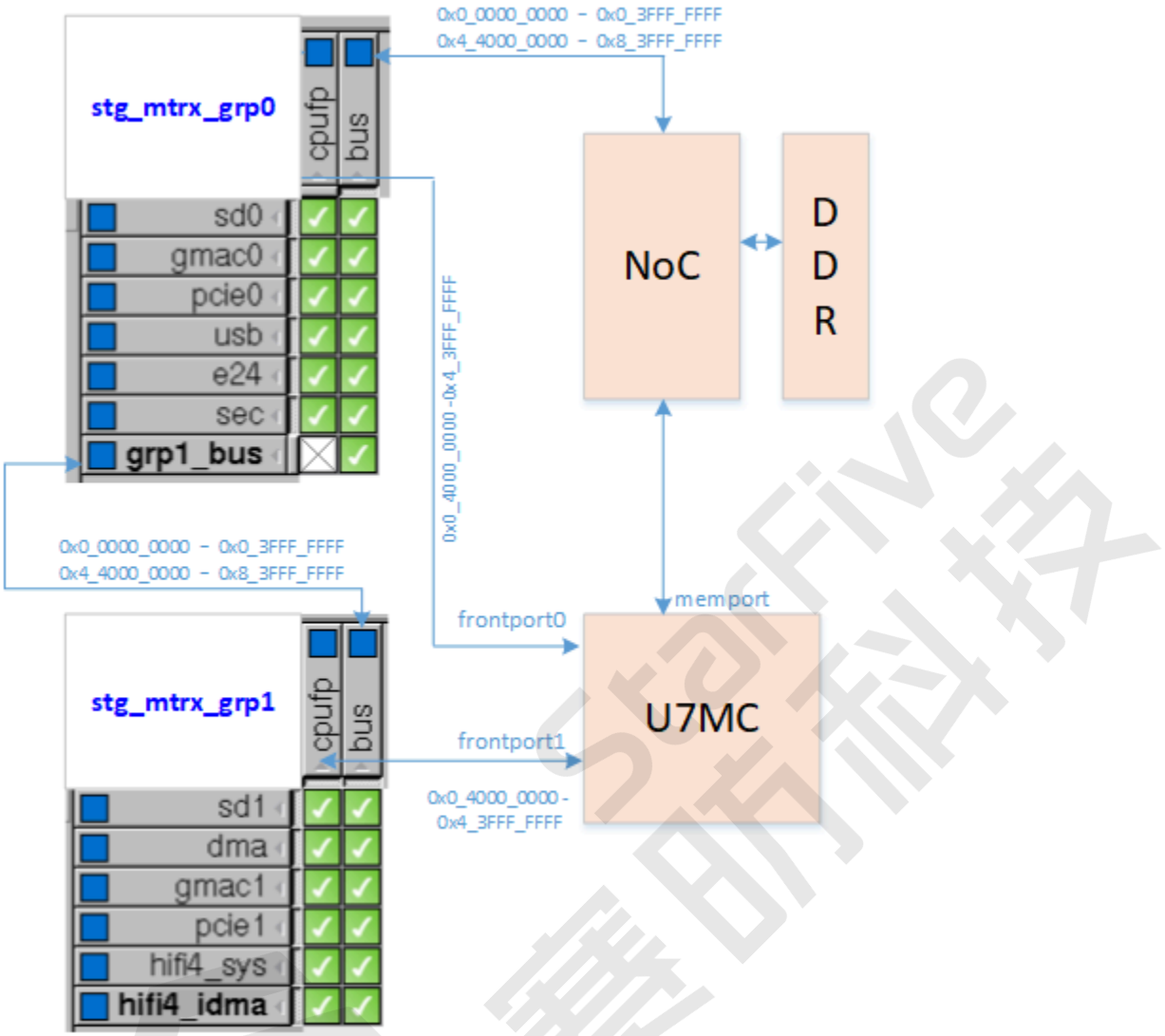
Table 2-1 System Bus Connection

OIC 18x8		Slave Port ID					
		OMC	axi_cfg0	axi_cfg1	apb_cfg0	apb_cfg1	orbit_cr1
Master Port ID	CPUSYS	0	0	X	X	X	X
	CPUPER	X	X	0	0	0	0
	CPUMEM	0	X	X	X	X	X
	GPU	0	X	X	X	X	X
	VDEC	0	X	X	X	X	X
	VENC	0	X	X	X	X	X
	VOUT0	0	X	X	X	X	X
	VOUT1	0	X	X	X	X	X
	ISP0	0	X	X	X	X	X
	STG	0	0	0	0	0	0

In the STG subsystem, system includes 2 bus inter-connectors. The connection and address offsets are displayed in the following diagram.

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Figure 2-2 Bus Connections in STG



2.2. Boot Process

The following table shows the boot process of JH-7110.

Table 2-2 System Boot Process

Processor	Boot Mode (PAD_RGPIO2)	Boot Vector	Boot Selection (PAD_RGPIO[1:0])
U74MC	0x1	0x00_2100_0000	XIP Flash
	0x0	0x00_2A00_0000	0x0: Boot from 1-bit QSPI instead of flash 0x1: Boot from SDIO3.0 0x2: Boot from EMMC5.1 0x3: Boot from UART
Audio DSP		Defined by U74MC or E24	
E24		Defined by U74MC	

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Note:

- If XIP flash is disabled in OTP configuration, system cannot boot from XIP flash.
- The On-Chip boot ROM is 32 KB.
- The boot mode and boot options could be loaded from the SYSCON status registers.

Boot Modes

System supports the following boot modes.

- Boot ROM
- QSPI NOR/NAND Flash
- SD card/eMMC
- UART/USB/SD CARD update

2.3. Interrupt

2.3.1. Interrupt Concepts

Interrupts are asynchronous events that cause program execution to change to a specific location in the software application to handle the interrupting event. When processing of the interrupt is complete, program execution resumes back to the original program execution location. For example, a timer that triggers every 10 milliseconds will cause the CPU to branch to the interrupt handler, acknowledge the interrupt, and set the next 10 millisecond interval.

The interrupt controller processes incoming interrupts by masking and priority sorting to produce the interrupt signals for the processor to which it is attached.

CLINT

Core Local Interrupter (CLINT) is intended to be used to generate Machine-level timer and software interrupts for the targeted Harts in a pre-integrated core subsystem.

PLIC

Platform-Level Interrupt Controller (PLIC) is intended to be used to manage all global interrupt sources as External Interrupts to a pre-integrated core subsystem.

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2.3.2. Interrupt Connections

The following table shows the interrupt connection of JH-7110.

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Table 2-3 System Interrupt Connections

Instance	IRQ Request	u0_u7mc_sft7110(clock)	u0_hifi4	u0_e2_sft7110(clock)	u0_int_ctrl
u0_gmac5_axi64	lpi_intr_o	global_interrupts[0]		local_interrupts_0[0]	int_src_in[0]
	pmt_intr_o	global_interrupts[1]		local_interrupts_0[1]	int_src_in[1]
	sbd_intr_o	global_interrupts[2]		local_interrupts_0[2]	int_src_in[2]
	sbd_tx_intr_o	global_interrupts[3]		local_interrupts_0[3]	int_src_in[3]
	sbd_rx_intr_o	global_interrupts[4]		local_interrupts_0[4]	int_src_in[4]
u0_rtc_hms	ms_pulse_o	global_interrupts[5]		local_interrupts_0[5]	int_src_in[5]
	one_sec_pulse_o	global_interrupts[6]		local_interrupts_0[6]	
	rtc_irq_o	global_interrupts[7]	BInterrupt[0]	local_interrupts_0[7]	
u0_WAVE511	o_vpu_intrpt	global_interrupts[8]		local_interrupts_0[8]	
u0_CODAJ12	o_intrpt_req	global_interrupts[9]		local_interrupts_0[9]	
u0_wave420l	o_vpu_intrpt	global_interrupts[10]		local_interrupts_0[10]	
u0_sft7110_noc_bus	oic_interrupts[0]	global_interrupts[11]		local_interrupts_0[11]	
	oic_interrupts[1]	global_interrupts[12]		local_interrupts_0[12]	
	oic_interrupts[2]	global_interrupts[13]		local_interrupts_0[13]	
u0_ddr_sft7110	ddrc_asp_int	global_interrupts[14]		local_interrupts_0[14]	int_src_in[6]
	ddrc_cooldown_int	global_interrupts[15]		local_interrupts_0[15]	int_src_in[7]
	ddrc_hightemp_int	global_interrupts[16]		local_interrupts_0[16]	int_src_in[8]
	ddrc_overtemp_int	global_interrupts[17]		local_interrupts_0[17]	int_src_in[9]
	ddrc_phy_int	global_interrupts[18]		local_interrupts_0[18]	int_src_in[10]
	phy0_freq_int	global_interrupts[19]		local_interrupts_0[19]	int_src_in[11]
u0_cdns_qspi	interrupt	global_interrupts[20]	BInterrupt[1]	local_interrupts_0[20]	int_src_in[12]
u0_mailbox	c0_to_c1_irq		BInterrupt[2]		
	c0_to_c2_irq			local_interrupts_0[21]	
	c0_to_c3_irq				

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Table 2-3 System Interrupt Connections (continued)

Instance	IRQ Request	u0_u7mc_sft7110(clock)	u0_hifi4	u0_e2_sft7110(clock)	u0_int_ctrl
	c1_to_c0_irq	global_interrupts[21]			
	c1_to_c2_irq			local_interrupts_0[22]	
	c1_to_c3_irq				
	c2_to_c0_irq	global_interrupts[22]			
	c2_to_c1_irq		BInterrupt[3]		
	c2_to_c3_irq				
	c3_to_c0_irq				
	c3_to_c1_irq				
	c3_to_c2_irq				
u0_sec_top	sec_algc_int	global_interrupts[23]	BInterrupt[4]	local_interrupts_0[23]	
	sec_dmac_int	global_interrupts[24]	BInterrupt[5]	local_interrupts_0[24]	
	sec_trng_int	global_interrupts[25]	BInterrupt[6]	local_interrupts_0[25]	
u0_otpc	otp_int	global_interrupts[26]	BInterrupt[7]	local_interrupts_0[26]	
u0_uart	intr	global_interrupts[27]	BInterrupt[8]	local_interrupts_0[27]	
u1_uart	intr	global_interrupts[28]		local_interrupts_0[28]	
u2_uart	intr	global_interrupts[29]		local_interrupts_0[29]	
u0_i2c	ic_intr	global_interrupts[30]	BInterrupt[9]	local_interrupts_0[30]	
u1_i2c	ic_intr	global_interrupts[31]	BInterrupt[10]	local_interrupts_0[31]	
u2_i2c	ic_intr	global_interrupts[32]		local_interrupts_0[32]	
u0_ssp_spi	SSPINTR	global_interrupts[33]	BInterrupt[11]	local_interrupts_0[33]	
u1_ssp_spi	SSPINTR	global_interrupts[34]		local_interrupts_0[34]	
u2_ssp_spi	SSPINTR	global_interrupts[35]		local_interrupts_0[35]	
		global_interrupts[36]		local_interrupts_0[36]	
u0_i2srx_3ch	rx_0_intr	global_interrupts[37]	BInterrupt[13]	local_interrupts_0[37]	

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Table 2-3 System Interrupt Connections (continued)

Instance	IRQ Request	u0_u7mc_sft7110(clock)	u0_hifi4	u0_e2_sft7110(clock)	u0_int_ctrl
	rx_1_intr	global_interrupts[38]	BInterrupt[14]	local_interrupts_0[38]	
	rx_2_intr	global_interrupts[39]	BInterrupt[15]	local_interrupts_0[39]	
u3_uart	intr	global_interrupts[40]		local_interrupts_0[40]	
u4_uart	intr	global_interrupts[41]		local_interrupts_0[41]	
u5_uart	intr	global_interrupts[42]		local_interrupts_0[42]	
u3_i2c	ic_intr	global_interrupts[43]		local_interrupts_0[43]	
u4_i2c	ic_intr	global_interrupts[44]		local_interrupts_0[44]	
u5_i2c	ic_intr	global_interrupts[45]		local_interrupts_0[45]	
u6_i2c	ic_intr	global_interrupts[46]		local_interrupts_0[46]	
u3_ssp_spi	SSPINTR	global_interrupts[47]		local_interrupts_0[47]	
u4_ssp_spi	SSPINTR	global_interrupts[48]		local_interrupts_0[48]	
u5_ssp_spi	SSPINTR	global_interrupts[49]		local_interrupts_0[49]	
u6_ssp_spi	SSPINTR	global_interrupts[50]		local_interrupts_0[50]	
u0_plda_pcie	local_interrupt	global_interrupts[51]		local_interrupts_0[51]	
u1_plda_pcie	local_interrupt	global_interrupts[52]		local_interrupts_0[52]	
u0_i2stx_4ch	intr	global_interrupts[53]	BInterrupt[16]	local_interrupts_0[53]	int_src_in[13]
u1_i2stx_4ch	intr	global_interrupts[54]	BInterrupt[17]	local_interrupts_0[54]	int_src_in[14]
u0_pwm_8ch	ptc_intr[0]	global_interrupts[55]	BInterrupt[18]	local_interrupts_0[55]	int_src_in[15]
	ptc_intr[1]	global_interrupts[56]		local_interrupts_0[56]	int_src_in[16]
	ptc_intr[2]	global_interrupts[57]		local_interrupts_0[57]	int_src_in[17]
	ptc_intr[3]	global_interrupts[58]		local_interrupts_0[58]	int_src_in[18]
	ptc_intr[4]	global_interrupts[59]		local_interrupts_0[59]	int_src_in[19]
	ptc_intr[5]	global_interrupts[60]		local_interrupts_0[60]	
	ptc_intr[6]	global_interrupts[61]		local_interrupts_0[61]	

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Table 2-3 System Interrupt Connections (continued)

Instance	IRQ Request	u0_u7mc_sft7110(clock)	u0_hifi4	u0_e2_sft7110(clock)	u0_int_ctrl
	ptc_intr[7]	global_interrupts[62]		local_interrupts_0[62]	
u0_dskit_wdt	WDOGINT	global_interrupts[63]	BInterrupt[12]	local_interrupts_0[63]	
u0_si5_timer	TIMER_INTR[0]	global_interrupts[64]	BInterrupt[19]	local_interrupts_0[64]	
	TIMER_INTR[1]	global_interrupts[65]		local_interrupts_0[65]	
	TIMER_INTR[2]	global_interrupts[66]		local_interrupts_0[66]	
	TIMER_INTR[3]	global_interrupts[67]		local_interrupts_0[67]	
u0_dma1p_8ch_56hs	intr	global_interrupts[68]	BInterrupt[20]	local_interrupts_0[68]	int_src_in[20]
u0_sdio	interrupt	global_interrupts[69]	BInterrupt[21]	local_interrupts_0[69]	int_src_in[21]
u1_sdio	interrupt	global_interrupts[70]		local_interrupts_0[70]	int_src_in[22]
u1_gmac5_axi64	lpi_intr_o	global_interrupts[71]		local_interrupts_0[71]	int_src_in[23]
	pmt_intr_o	global_interrupts[72]		local_interrupts_0[72]	int_src_in[24]
	sbd_intr_o	global_interrupts[73]		local_interrupts_0[73]	int_src_in[25]
	sbd_tx_intr_o	global_interrupts[74]		local_interrupts_0[74]	int_src_in[26]
	sbd_rx_intr_o	global_interrupts[75]		local_interrupts_0[75]	int_src_in[27]
u0_temp_sensor	tempsense_int	global_interrupts[76]		local_interrupts_0[76]	int_src_in[28]
u0_img_gpu	gpu_os_irq	global_interrupts[77]		local_interrupts_0[77]	int_src_in[29]
	gpu_pow_gpio_irq	global_interrupts[78]		local_interrupts_0[78]	int_src_in[30]
u0_cdns_spdif	intreq	global_interrupts[79]		local_interrupts_0[79]	int_src_in[31]
u0_aon_iomux	gpio_irq	global_interrupts[80]	BInterrupt[22]	local_interrupts_0[80]	int_src_in[32]
u0_sys_iomux	gpio_irq	global_interrupts[81]	BInterrupt[23]	local_interrupts_0[81]	int_src_in[33]
u0_dom_isp_top	u0_ispv2_top_wrapper_isp_interrupt_out[0]	global_interrupts[82]		local_interrupts_0[82]	int_src_in[34]
	u0_ispv2_top_wrapper_isp_interrupt_out[1]	global_interrupts[83]		local_interrupts_0[83]	int_src_in[35]

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Table 2-3 System Interrupt Connections (continued)

Instance	IRQ Request	u0_u7mc_sft7110(clock)	u0_hifi4	u0_e2_sft7110(clock)	u0_int_ctrl
	u0_ispv2_top_wrapper_isp_interrupt_out[2]	global_interrupts[84]		local_interrupts_0[84]	int_src_in[36]
	u0_ispv2_top_wrapper_isp_interrupt_out[3]	global_interrupts[85]		local_interrupts_0[85]	int_src_in[37]
	u0_vin_AXIRD_INTR	global_interrupts[86]		local_interrupts_0[86]	int_src_in[38]
	u0_vin_AXIWR0_INTR	global_interrupts[87]		local_interrupts_0[87]	int_src_in[39]
	u0_vin_irq	global_interrupts[88]		local_interrupts_0[88]	int_src_in[40]
	u0_vin_err_irq	global_interrupts[89]		local_interrupts_0[89]	int_src_in[41]
u0_dom_vout_top	vout_sys_int[0]	global_interrupts[90]		local_interrupts_0[90]	int_src_in[42]
	vout_sys_int[1]	global_interrupts[91]		local_interrupts_0[91]	int_src_in[43]
	vout_sys_int[2]	global_interrupts[92]		local_interrupts_0[92]	int_src_in[44]
	vout_sys_int[3]	global_interrupts[93]		local_interrupts_0[93]	int_src_in[45]
	vout_sys_int[4]	global_interrupts[94]		local_interrupts_0[94]	int_src_in[46]
u0_cdn_usb	interrupt_req[0]	global_interrupts[95]		local_interrupts_0[95]	int_src_in[47]
	interrupt_req[1]	global_interrupts[96]		local_interrupts_0[96]	int_src_in[48]
	interrupt_req[2]	global_interrupts[97]		local_interrupts_0[97]	int_src_in[49]
	interrupt_req[3]	global_interrupts[98]		local_interrupts_0[98]	int_src_in[50]
	interrupt_req[4]	global_interrupts[99]		local_interrupts_0[99]	int_src_in[51]
	interrupt_req[5]	global_interrupts[100]		local_interrupts_0[100]	int_src_in[52]
	interrupt_req[6]	global_interrupts[101]		local_interrupts_0[101]	int_src_in[53]
	interrupt_req[7]	global_interrupts[102]		local_interrupts_0[102]	int_src_in[54]
	irqs[0]	global_interrupts[103]		local_interrupts_0[103]	int_src_in[55]
	irqs[1]	global_interrupts[104]		local_interrupts_0[104]	int_src_in[56]
	otgirq	global_interrupts[105]		local_interrupts_0[105]	
u0_pmu	irq_o	global_interrupts[106]	BInterrupt[24]	local_interrupts_0[106]	int_src_in[57]

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Table 2-3 System Interrupt Connections (continued)

Instance	IRQ Request	u0_u7mc_sft7110(clock)	u0_hifi4	u0_e2_sft7110(clock)	u0_int_ctrl
u0_can_ctrl	host_irq	global_interrupts[107]		local_interrupts_0[107]	int_src_in[58]
u1_can_ctrl	host_irq	global_interrupts[108]		local_interrupts_0[108]	int_src_in[59]
u0_int_ctrl	intc_irq_0	global_interrupts[109]		local_interrupts_0[109]	
		global_interrupts[110]		local_interrupts_0[110]	
		global_interrupts[111]		local_interrupts_0[111]	
		global_interrupts[112]		local_interrupts_0[112]	
		global_interrupts[113]		local_interrupts_0[113]	
		global_interrupts[114]		local_interrupts_0[114]	
		global_interrupts[115]		local_interrupts_0[115]	
		global_interrupts[116]		local_interrupts_0[116]	
		global_interrupts[117]		local_interrupts_0[117]	
		global_interrupts[118]		local_interrupts_0[118]	
		global_interrupts[119]		local_interrupts_0[119]	
		global_interrupts[120]		local_interrupts_0[120]	
		global_interrupts[121]		local_interrupts_0[121]	
		global_interrupts[122]		local_interrupts_0[122]	
		global_interrupts[123]		local_interrupts_0[123]	int_src_in[60]
		global_interrupts[124]		local_interrupts_0[124]	int_src_in[61]
		global_interrupts[125]		local_interrupts_0[125]	int_src_in[62]
		global_interrupts[126]		local_interrupts_0[126]	int_src_in[63]
				meip_0	

2.4. Memory Map

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2.4.1. System Memory Map

The following table shows the memory map of the JH-7110 system.

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Table 2-4 System Memory Map

Start Address	End Address	Size	Attribute	Device/Description
0x00_1000_0000	0x00_1000_FFFF	64KB	RW A	UART0
0x00_1001_0000	0x00_1001_FFFF	64KB	RW A	UART1
0x00_1002_0000	0x00_1002_FFFF	64KB	RW A	UART2
0x00_1003_0000	0x00_1003_FFFF	64KB	RW A	I2C0
0x00_1004_0000	0x00_1004_FFFF	64KB	RW A	I2C1
0x00_1005_0000	0x00_1005_FFFF	64KB	RW A	I2C2
0x00_1006_0000	0x00_1006_FFFF	64KB	RW A	SPI0
0x00_1007_0000	0x00_1007_FFFF	64KB	RW A	SPI1
0x00_1008_0000	0x00_1008_FFFF	64KB	RW A	SPI2
0x00_1009_0000	0x00_1009_FFFF	64KB	RW A	TMD_16SLOT_APB
0x00_100A_0000	0x00_100A_FFFF	64KB	RW A	SPDIF
0x00_100B_0000	0x00_100B_FFFF	64KB	RW A	PWMDAC
0x00_100D_0000	0x00_100D_FFFF	64KB	RW A	PDM4MIC
0x00_100E_0000	0x00_100E_FFFF	64KB	RW A	I2SRX_3CH
0x00_100F_0000	0x00_100F_FFFF	64KB	RW A	Reserved
0x00_1010_0000	0x00_101F_FFFF	1MB	RW A	USB Controller
0x00_1020_0000	0x00_1020_FFFF	64KB	RW A	USB2.0 UITMI PHY
0x00_1021_0000	0x00_1021_FFFF	64KB	RW A	PCIE0 PHY
0x00_1022_0000	0x00_1022_FFFF	64KB	RW A	PCIE1 PHY
0x00_1023_0000	0x00_1023_FFFF	64KB	RW A	STG_CRG
0x00_1024_0000	0x00_1024_FFFF	64KB	RW A	STG_SYSCON
0x00_1025_0000	0x00_11FF_FFFF			Reserved
0x00_1200_0000	0x00_1200_FFFF	64KB	RW A	UART3
0x00_1201_0000	0x00_1201_FFFF	64KB	RW A	UART4

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Table 2-4 System Memory Map (continued)

Start Address	End Address	Size	Attribute	Device/Description
0x00_1202_0000	0x00_1202_FFFF	64KB	RW A	UART5
0x00_1203_0000	0x00_1203_FFFF	64KB	RW A	I2C3
0x00_1204_0000	0x00_1204_FFFF	64KB	RW A	I2C4
0x00_1205_0000	0x00_1205_FFFF	64KB	RW A	I2C5
0x00_1206_0000	0x00_1206_FFFF	64KB	RW A	I2C6
0x00_1207_0000	0x00_1207_FFFF	64KB	RW A	SPI3
0x00_1208_0000	0x00_1208_FFFF	64KB	RW A	SPI4
0x00_1209_0000	0x00_1209_FFFF	64KB	RW A	SPI5
0x00_120A_0000	0x00_120A_FFFF	64KB	RW A	SPI6
0x00_120B_0000	0x00_120B_FFFF	64KB	RW A	I2STX_4CH 0
0x00_120C_0000	0x00_120C_FFFF	64KB	RW A	I2STX_4CH 1
0x00_120D_0000	0x00_120D_FFFF	64KB	RW A	PWM_8CH
0x00_120E_0000	0x00_120E_FFFF	64KB	RW A	Temperature sensor
0x00_120F_0000	0x00_12FF_FFFF			Reserved
0x00_1300_0000	0x00_1300_FFFF	64KB	RW A	DDR PHY
0x00_1301_0000	0x00_1301_FFFF	64KB	RW A	QSPI CSR
0x00_1302_0000	0x00_1302_FFFF	64KB	RW A	System CRG
0x00_1303_0000	0x00_1303_FFFF	64KB	RW A	System SYSCON
0x00_1304_0000	0x00_1304_FFFF	64KB	RW A	System IOMUX
0x00_1305_0000	0x00_1305_FFFF	64KB	RW A	Timer
0x00_1306_0000	0x00_1306_FFFF	64KB	RW A	Mailbox
0x00_1307_0000	0x00_1307_FFFF	64KB	RW A	WDT
0x00_1308_0000	0x00_1308_FFFF	64KB	RW A	INTC
0x00_1309_0000	0x00_1309_FFFF	64KB	RW A	JPEG Codec

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Table 2-4 System Memory Map (continued)

Start Address	End Address	Size	Attribute	Device/Description
0x00_130A_0000	0x00_130A_FFFF	64KB	RW A	Video decoder
0x00_130B_0000	0x00_130B_FFFF	64KB	RW A	Video encoder
0x00_130C_0000	0x00_130C_FFFF	64KB	RW A	GPU timer
0x00_130D_0000	0x00_130D_FFFF	64KB	RW A	CAN0(2.0B)
0x00_130E_0000	0x00_130E_FFFF	64KB	RW A	CAN1(2.0B)
0x00_1310_0000	0x00_14FF_FFFF			Reserved
0x00_1500_0000	0x00_156F_FFFF	16MB	RW A	NOC Bus CSR
0x00_1570_0000	0x00_1570_FFFF	64KB	RW A	DDRC
0x00_1571_0000	0x00_15FF_FFFF			Reserved
0x00_1600_0000	0x00_1600_FFFF	16KB	RW A	Security subsystem
0x00_1600_0000	0x00_1600_3FFF	16KB	RW A	Security algorithm
0x00_1600_4000	0x00_1600_7FFF	16KB	RW A	Reserved
0x00_1600_8000	0x00_1600_BFFF	16KB	RW A	Security DMA
0x00_1600_C000	0x00_1600_FFFF	16KB	RW A	TRNG
0x00_1601_0000	0x00_1601_FFFF	64KB	RW A	SDIO0
0x00_1602_0000	0x00_1602_FFFF	64KB	RW A	SDIO1
0x00_1603_0000	0x00_1603_FFFF	64KB	RW A	GMAC0
0x00_1604_0000	0x00_1604_FFFF	64KB	RW A	GMAC1
0x00_1605_0000	0x00_1605_FFFF	64KB	RW A	DW_DMAC
0x00_1606_0000	0x00_1607_FFFF	64KB	RW A	Reserved
0x00_1608_0000	0x00_16FF_FFFF	64KB	RW A	Reserved
0x00_1700_0000	0x00_1700_FFFF	64KB	RW A	AON CRG
0x00_1701_0000	0x00_1701_FFFF	64KB	RW A	AON SYSCON
0x00_1702_0000	0x00_1702_FFFF	64KB	RW A	AON GPIO

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Table 2-4 System Memory Map (continued)

Start Address	End Address	Size	Attribute	Device/Description
0x00_1703_0000	0x00_1703_FFFF	64KB	RW A	PMU
0x00_1704_0000	0x00_1704_FFFF	64KB	RW A	RTC_HMS
0x00_1705_0000	0x00_1705_FFFF	64KB	RW A	OTPC
0x00_1706_0000	0x00_170B_FFFF			Reserved
0x00_170C_0000	0x00_170C_FFFF	64KB	RW A	TDM16SLOT_AHB
0x00_170D_0000	0x00_17FF_FFFF			Reserved
0x00_1800_0000	0x00_180F_FFFF	1MB	RW A	GPU
0x00_1810_0000	0x00_197F_FFFF			Reserved
0x00_1980_0000	0x00_1980_FFFF	64KB	RW A	MIPI_CSI_CTRL0
0x00_1981_0000	0x00_1981_FFFF	64KB	RW A	DOM_ISP_CRG
0x00_1982_0000	0x00_1982_FFFF	64KB	RW A	MIPIRX_DPHY APB configuration
0x00_1984_0000	0x00_1984_FFFF	64KB	RW A	DOM_ISP_SYSCON
0x00_1985_0000	0x00_1986_FFFF			Reserved
0x00_1987_0000	0x00_1989_FFFF	384KB	RW A	ISPV1_MINI
0x00_198A_0000	0x00_1FFF_FFFF			Reserved
0x00_2000_0000	0x00_2000_7FFF			Reserved
0x00_2000_8000	0x00_2000_FFFF	32KB	RWX	Audio DSP DRAM1, remap to 0x4000_8000
0x00_2001_0000	0x00_2001_FFFF	64KB	RWX	Audio DSP DRAM0, remap to 0x4001_0000
0x00_2002_0000	0x00_2002_FFFF	64KB	RWX	Audio DSP IRAM0, remap to 0x4002_0000
0x00_2003_0000	0x00_2003_7FFF	32KB	RWX	Audio DSP IRAM1, remap to 0x4003_0000
0x00_2003_8FFF	0x00_20FF_FFFF			Reserved
0x00_2100_0000	0x00_28FF_FFFF	128MB	RWX	QSPI XIP memory, AHB slave
0x00_2900_0000	0x00_293F_FFFF			Reserved
0x00_2940_0000	0x00_2947_FFFF	512KB	RW	DC8200 AHB0

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Table 2-4 System Memory Map (continued)

Start Address	End Address	Size	Attribute	Device/Description
0x00_2948_0000	0x00_294F_FFFF	512KB	RW	DC8200 AHB1
0x00_2950_0000	0x00_2958_FFFF			Reserved
0x00_2959_0000	0x00_2959_FFFF	64KB	RW	U0_HDMITX
0x00_295A_0000	0x00_295A_FFFF			Reserved
0x00_295B_0000	0x00_295B_FFFF	64KB	RW	VOUT_SYSCON
0x00_295C_0000	0x00_295C_FFFF	64KB	RW	VOUT_CRG
0x00_295D_0000	0x00_295D_FFFF	64KB	RW	DSI TX
0x00_295E_0000	0x00_295E_FFFF	64KB	RW	MIPITX DPHY configuration
0x00_295F_0000	0x00_29FF_FFFF			Reserved
0x00_2A00_0000	0x00_2A00_81FF	32KB	RX	Boot ROM
0x00_2A01_0000	0x00_2AFF_FFFF			Reserved
0x00_2B00_0000	0x00_2BFF_FFFF	16MB	RW	PCIE0 controller CSR
0x00_2C00_0000	0x00_2CFF_FFFF	16MB	RW	PCIE1 controller CSR
0x00_2D00_0000	0x00_3FFF_FFFF			Reserved
0x00_3000_0000	0x00_37FF_FFFF	128MB	RW	PCIE0 memory space for 32-bit devices
0x00_3800_0000	0x00_3FFF_FFFF	128MB	RW	PCIE1 memory space for 32-bit devices
0x00_4000_0000	0x02_3FFF_FFFF	8GB	RWX C A N	DDR for memory port
0x02_4000_0000	0x04_3FFF_FFFF	8GB		Reserved
0x04_4000_0000	0x06_3FFF_FFFF	8GB	RWX N	DDR for system port
0x06_4000_0000	0x08_3FFF_FFFF	8GB		Reserved
0x09_0000_0000	0x09_3FFF_FFFF	1GB	RW	PCIE0 memory space,start address & size are both configurable
0x09_4000_0000	0x09_4FFF_FFFF	256MB	RW	PCIE0 configuration space,start address is configurable,size is fixed

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Table 2-4 System Memory Map (continued)

Start Address	End Address	Size	Attribute	Device/Description
0x09_8000_0000	0x09_BFFF_FFFF	1GB	RW	PCIE1 memory space,start address & size are both configurable
0x09_C000_0000	0x09_CFFF_FFFF	256MB	RW	PCIE1 configuration space,start address is configurable,size is fixed

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2.4.2. U74 Memory Map

The following table shows the memory map of U74 Core Complex.

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Table 2-5 U74 Memory Map

Start Address	End Address	Size	Attribute	Device
0x00_0000_0000	0x00_0000_00FF			Debug
0x00_0000_0100	0x00_0000_2FFF			Reserved
0x00_0000_3000	0x00_0000_3FFF		RWX A	Error Device
0x00_0000_4000	0x00_015F_FFFF			Reserved
0x00_0110_1000	0x00_0110_1FFF	8KB	RWX A	S7 Hart0 DTIM
0x00_0170_0000	0x00_0170_0FFF		RW A	S7 Hart0 Bus-Error Unit
0x00_0170_1000	0x00_0170_1FFF		RW A	U7 Hart1 Bus-Error Unit
0x00_0170_2000	0x00_0170_2FFF		RW A	U7 Hart2 Bus-Error Unit
0x00_0170_3000	0x00_0170_3FFF		RW A	U7 Hart3 Bus-Error Unit
0x00_0170_4000	0x00_0170_4FFF		RW A	U7 Hart3 Bus-Error Unit
0x00_0170_5000	0x00_01FF_FFFF			Reserved
0x00_0200_0000	0x00_0200_FFFF		RW A	CLINT
0x00_0201_0000	0x00_0201_3FFF		RW A	L2 Cache controller
0x00_0201_4000	0x00_0203_1FFF			Reserved
0x00_0203_2000	0x00_0203_3FFF		RW A	U7 Hart1 L2 Prefetcher
0x00_0203_4000	0x00_0203_5FFF		RW A	U7 Hart2 L2 Prefetcher
0x00_0203_6000	0x00_0203_7FFF		RW A	U7 Hart3 L2 Prefetcher
0x00_0203_8000	0x00_0203_9FFF		RW A	U7 Hart4 L2 Prefetcher
0x00_0203_A000	0x00_07FF_FFFF			Reserved
0x00_0800_0000	0x00_081F_FFFF		RWX A	L2 LIM
0x00_0820_0000	0x00_09FF_FFFF		RW A	Reserved
0x00_0A00_0000	0x00_0A1F_FFFF		RWX I A	L2 Zero Device
0x00_0A20_0000	0x00_0BFF_FFFF			Reserved
0x00_0C00_0000	0x00_0FFF_FFFF		RW A	PLIC

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Table 2-5 U74 Memory Map (continued)

Start Address	End Address	Size	Attribute	Device
0x00_0000_0000	0x00_0FFF_FFFF			U74 internal
0x00_1000_0000	0x00_1FFF_FFFF	256MB		Peripheral port
0x00_2000_0000	0x00_3FFF_FFFF	512MB	RWX A	System port
0x00_4000_0000	0x04_3FFF_FFFF	16GB		Memory port
0x04_4000_0000	0x08_3FFF_FFFF	16GB	RW A	System port
0x09_0000_0000	0x09_7FFF_FFFF	2GB	RWX A	System port
0x09_8000_0000	0x09_FFFF_FFFF	2GB	RWX A	PCIE configuration space + memory space

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2.4.3. E24 Memory Map

The following table shows the memory map of E24 Core Complex.

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Table 2-6 E24 Memory Map

Start Address	End Address	Size	Attribute	Device
0x0000_0000	0x0000_00FF			Debug
0x0000_0100	0x0000_2FFF			Reserved
0x0000_3000	0x0000_3FFF		RWX A	Error Device
0x0000_4000	0x015F_FFFF			Reserved
0x0200_0000	0x0200_FFFF		RW A	CLINT
0x1000_0000	0x3FFF_FFFF	1G-128MB	RW A	Peripheral
0x4000_0000	0xFFFF_FFFF	3GB	RWX C A	DDR, could be remapped to other 3GB space through SYSCON

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2.4.4. Audio DSP Memory Map

The following table shows the memory map of Audio DSP.

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Table 2-7 Audio DSP Memory Map

Start Address	End Address	Size	Attribute	Device
0x0000_0000	0x0FFF_FFFF	128MB		Reserved
0x1000_0000	0x3FFF_FFFF	256MB	RW A	Peripheral & Memory
0x4000_8000	0x4000_FFFF	32KB	RWX C A	Data RAM1
0x4001_0000	0x4001_FFFF	64KB	RWX C A	Data RAM0
0x4002_0000	0x4002_FFFF	64KB	RWX C A	Instruction RAM0
0x4003_0000	0x4003_7FFF	32KB	RWX C A	Instruction RAM1
0x4100_0000	0xFFFF_FFFF		RWX C A	DDR, could be remapped to other 3GB space thru SYS-CON

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2.4.5. NoC Memory Map

The following table shows the memory map of NoC.

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Table 2-8 NoC Memory Map

Start Address	End Address	Size	Attribute	Device
0x1500_0000	0x1500_FFFF	64 KB	RW A	CNODE_MST00.CR
0x1502_0000	0x1502_FFFF	64 KB	RW A	RTMON_MST00.CR
0x1504_0000	0x1504_FFFF	64 KB	RW A	CNODE_MST01.CR
0x1506_0000	0x1506_FFFF	64 KB	RW A	RTMON_MST01.CR
0x1507_0000	0x1507_FFFF	64 KB	RW A	EVMON_MST01.CR
0x1508_0000	0x1508_FFFF	64 KB	RW A	CNODE_MST03.CR
0x150a_0000	0x150a_FFFF	64 KB	RW A	RTMON_MST03.CR
0x150e_0000	0x150e_FFFF	64 KB	RW A	BEMON_MST17.CR
0x1510_0000	0x1510_FFFF	64 KB	RW A	CNODE_MST02.CR
0x1511_0000	0x1511_FFFF	64 KB	RW A	FIRDR_MST02.CR
0x1512_0000	0x1512_FFFF	64 KB	RW A	RTMON_MST02.CR
0x1513_0000	0x1513_FFFF	64 KB	RW A	EVMON_MST02.CR
0x1514_0000	0x1514_FFFF	64 KB	RW A	CNODE_MST04.CR
0x1516_0000	0x1516_FFFF	64 KB	RW A	BEMON_MST04.CR
0x151b_0000	0x151b_FFFF	64 KB	RW A	EVMON_MST09.CR
0x152d_0000	0x152d_FFFF	64 KB	RW A	FIRDR_MST06.CR
0x152e_0000	0x152e_FFFF	64 KB	RW A	RTMON_MST06.CR
0x152f_0000	0x152f_FFFF	64 KB	RW A	EVMON_MST06.CR
0x1536_0000	0x1536_FFFF	64 KB	RW A	BEMON_MST08.CR
0x1537_0000	0x1537_FFFF	64 KB	RW A	EVMON_MST08.CR
0x153a_0000	0x153a_FFFF	64 KB	RW A	BEMON_MST09.CR
0x1542_0000	0x1542_FFFF	64 KB	RW A	FIRDR_MST10.CR
0x1543_0000	0x1543_FFFF	64 KB	RW A	EVMON_MST10.CR
0x1546_0000	0x1546_FFFF	64 KB	RW A	FIRDR_MST11.CR

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Table 2-8 NoC Memory Map (continued)

Start Address	End Address	Size	Attribute	Device
0x1547_0000	0x1547_FFFF	64 KB	RW A	EVMON_MST11.CR
0x1549_0000	0x1549_FFFF	64 KB	RW A	FIRDR_MST12.CR
0x154a_0000	0x154a_FFFF	64 KB	RW A	RTMON_MST12.CR
0x154b_0000	0x154b_FFFF	64 KB	RW A	EVMON_MST12.CR
0x154c_0000	0x154c_FFFF	64 KB	RW A	FIRDR_MST13.CR
0x154e_0000	0x154e_FFFF	64 KB	RW A	RTMON_MST13.CR
0x154f_0000	0x154f_FFFF	64 KB	RW A	EVMON_MST13.CR
0x1551_0000	0x1551_FFFF	64 KB	RW A	FIRDR_MST14.CR
0x1552_0000	0x1552_FFFF	64 KB	RW A	RTMON_MST14.CR
0x1553_0000	0x1553_FFFF	64 KB	RW A	EVMON_MST14.CR
0x1555_0000	0x1555_FFFF	64 KB	RW A	FIRDR_MST15.CR
0x1556_0000	0x1556_FFFF	64 KB	RW A	RTMON_MST15.CR
0x1557_0000	0x1557_FFFF	64 KB	RW A	EVMON_MST15.CR
0x1560_0000	0x1560_FFFF	64 KB	RW A	EVMON_SLV00.CR
0x1561_0000	0x1561_FFFF	64 KB	RW A	SNODE_SLV00.CR
0x1568_0000	0x1568_FFFF	64 KB	RW A	INTRRPT_DDR.CR
0x156a_0000	0x156a_FFFF	64 KB	RW A	SNODE_SLV01.CR
0x156c_0000	0x156c_FFFF	64 KB	RW A	INTRRPT_SYS.CR
0x156d_0000	0x156d_FFFF	64 KB	RW A	SNODE_SLV02.CR
0x156f_0000	0x156f_FFFF	64 KB	RW A	INTRRPT_ISP.CR
0x1570_0000	0x1570_FFFF	64 KB	RW A	OMC configuration and DDR control

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2.5. Clock and Reset

2.5.1. Reset Source

System includes the following reset sources.

Table 2-9 Reset Source

Source	Description
Pad	Used to reset the whole chip.
Watchdog	Used to reset the whole chip and all outputs to PAD.
Software reset in system top	Used to reset all logic modules except the “always-on” domain.
Software reset in the “always-on” domain	Used to reset the whole chip.
Low power **rstn**	Used to reset each power domain separately.

2.5.2. Reset Sequence

Follow the sequence below to reset the JH-7110 system.

Table 2-10 Reset Sequence

Sequence	Description
1	Powering up the chip, resetting the pad to active, and then latching the boot selection signals. The reset sequence starts after pad is reset to high.
2	5us delay, release the always-on domain reset, and clocks generated in always-on domain. And release the reset source on **dom_sys_top**.
3	Power down the PLL with 2us time interval
4	After the PLL power-down has been finished, wait 200us for PLL locking.
5	64 cycles of oscillator clock delay, release the system *Clock and Reset Generator (CRG)*'s reset to prepare the clock for system
6	64 cycles of oscillator clock delay, and release the system bus reset
7	Release CPU core reset after 32 cycles of oscillator clock delay has been completed. And CPU will boot from the boot vector.

2.5.3. Reset Process

Perform the following processes to reset the JH-7110 system.

Block	Function
reset_ctrl	1. Use this block to add a reset source and then sync it using **rstn_sync**. 2. Use this block to delay the reset for PLL lock, clock stabilization or other purposes. The delay time is configurable. 3. Use this block to release the reset for CPU, bus, a certain peripheral, or other modules. In this case, the block is used to release the reset and output **core_rstn** to **rstGen**. So, **core_rstn** is used to reset the whole digital logic module.

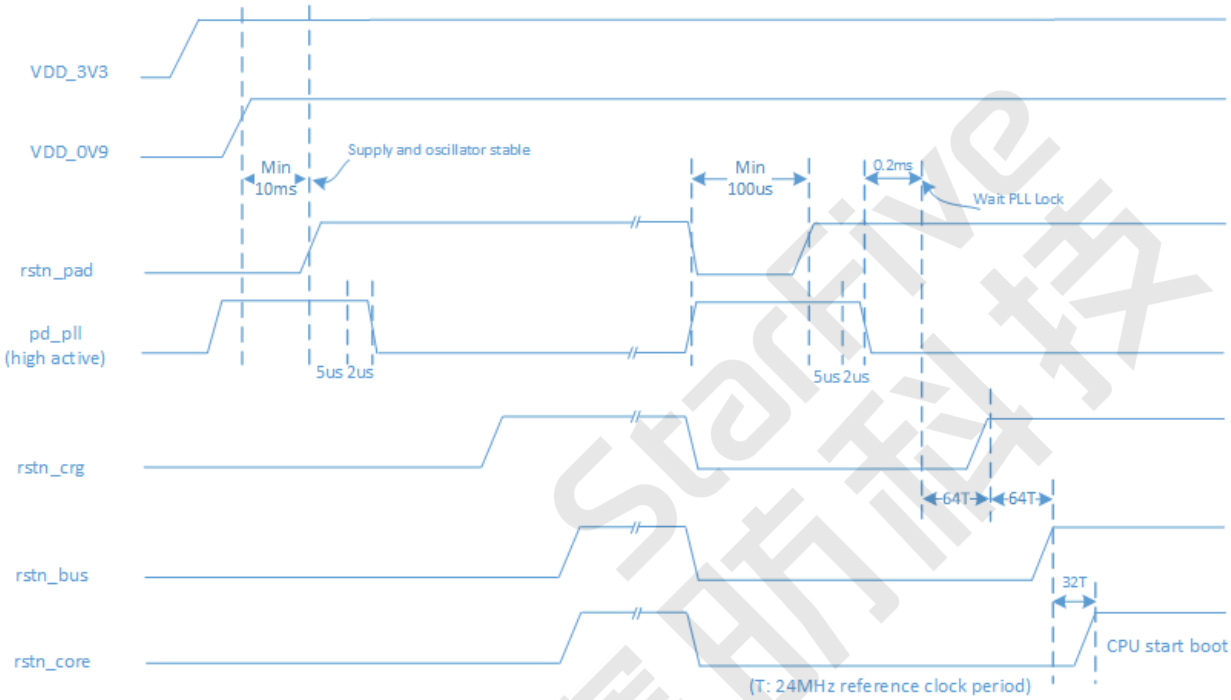
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Block	Function
rstgen	Use this block to control the software reset and synchronize the **rstn** added by hardware reset and software reset.

2.5.4. Reset Timing

The system PAD reset follows the timing sequence as described in the following diagram.

Figure 2-3 Reset Timing

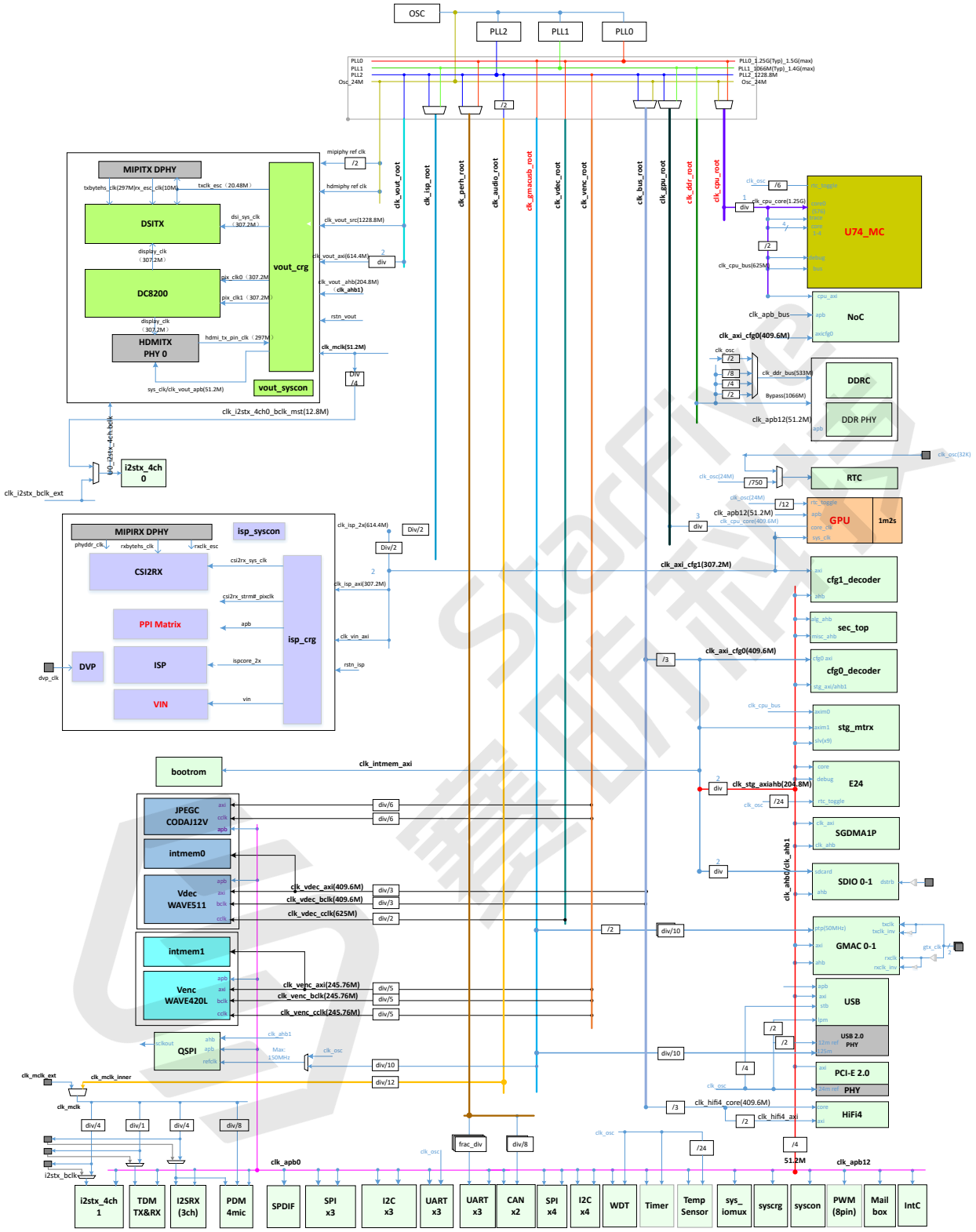


2.5.5. Clock Structure

The clock and reset structure of JH-7110 is displayed in the following diagram.

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Figure 2-4 Clock Structure



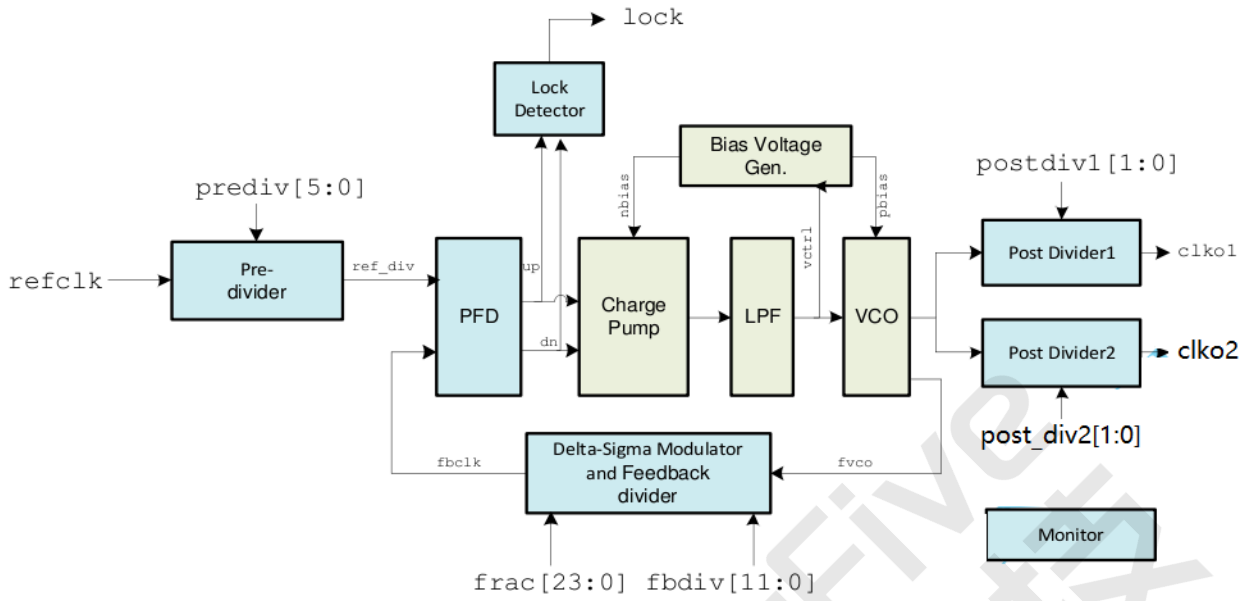
2.5.6. System PLL

JH-7110 system includes 3 PLLs, and the REFCLK is 24 MHz from external crystal.

The PLL clock frequency block diagram is shown in the following diagram.

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Figure 2-5 System PLL



PLL supports integer and fraction multiple, you should set **dacpd** and **dsmpd** to high while integer multiple mode, and set both them to low while fraction multiple mode.

Inter Multiple Mode

Both **dacpd** and **dsmpd** should be set as 1 while integer multiple mode.

The frequency of outputs can be figured out as below.

Fvco = Fref × NI ÷ M

NI is integer frequency dividing ratio of feedback divider, set by fbdiv[1:0] , NI = 8, 9, 10, 12, 13, …, 4095

M is frequency dividing ratio of pre-divider, set by prediv[5:0], M = 1, 2, …, 63

Fclkol = Fvco ÷ Ql

Q1 is frequency dividing ratio of post divider, set by postdiv[l:0], Ql = 1, 2, 4, 8

Fclko2 = Fvco ÷ Q2

Q2 is frequency dividing ratio of post divider, set by postdiv2[l:0], Q2= 1, 2, 4, 8

Fraction Multiple Mode

Both **dacpd** and **dsmpd** should be set as 0 while integer multiple mode.

Fvco = Fref × (NI+NF)÷M

NI is integer frequency dividing ratio of feedback divider, set by fbdivf 11:0] , NI = 8, 9, 10, 12, 13, …, 4095

NF is fractional frequency dividing ratio, set by frac[0:23]. NF =frac[0:23]/2^24 = 0 - 0.99999994

M is frequency dividing ratio of pre-divider, set by prediv[5:0], M = 1, 2, …, 63

Fclkol = Fvco ÷ Ql

Ql is frequency dividing ratio of post divider, set by postdivl [1:0],Q1 = 1, 2, 4, 8

Fclko2 = Fvco ÷ Q2

Q2 is frequency dividing ratio of post divider, set by postdiv2[1:0],Q2= 1, 2, 4, 8

2.5.7. Clock Specification

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The clock specification of JH-7110 is displayed in the following table.

Table 2-12 Clock Specifications

Module	Max (MHz)	Comment
U74	1,500	
GPU	400	
DDR	1,400	
JPEG Codec	200	
Video Decoder	400	
Video Encoder	250	
SGDMA	200	
AHB	200	
APB	50	
Display AXI	600	
MIPI and HDMI Pixel Clock	297	4K-30fps
LCD	74.25	1080p-30fps
ISP	300	
PCI-E	200	
USB	200	

2.6. Signal Description

The following table displays the system signals of JH-7110, including Pull-Up (PU) and Pull-Down (PD) settings.

Note:
The maximum current that a GPIO pin can afford is 3 A.

Note:
The following table only displays the default Pull-Up and Pull-Down settings of a signal. By writing 0 (No) or 1 (Yes) to the following signals, most of the PU/PD settings are configurable. "Tied to" means the PU PD settings of the signal are fixed, and not configurable.

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Table 2-13 System Signal Description

Signal Name	Description	PU	PD
TESTEN	Test Enable Signal Negative	Tied to 0	Tied to 1
RGPIO0	RGPIO0	0	0
RGPIO1	RGPIO1	0	0
RGPIO2	RGPIO2	0	0
RGPIO3	RGPIO3	0	1
SD_SEL18	SD Select 18	0	1
QSPI_SEL18	QSPI Select 18	1	0
GPIO0	GPIO0	0	0
GPIO1	GPIO1	1	0
GPIO2	GPIO2	0	0
GPIO3	GPIO3	0	0
GPIO4	GPIO4	1	0
GPIO5	GPIO5	1	0
GPIO6	GPIO6	1	0
GPIO7	GPIO7	0	0
GPIO8	GPIO8	0	0
GPIO9	GPIO9	1	0
GPIO10	GPIO10	0	0
GPIO11	GPIO11	0	0
GPIO12	GPIO12	1	0
GPIO13	GPIO13	1	0
GPIO14	GPIO14	0	0
GPIO15	GPIO15	0	0
GPIO16	GPIO16	0	0
GPIO17	GPIO17	0	0
GPIO18	GPIO18	1	0
GPIO19	GPIO19	1	0
GPIO20	GPIO20	0	0
GPIO21	GPIO21	0	0
GPIO22	GPIO22	0	0
GPIO23	GPIO23	0	0
GPIO24	GPIO24	0	0
GPIO25	GPIO25	0	0
GPIO26	GPIO26	0	0

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Table 2-13 System Signal Description (continued)

Signal Name	Description	PU	PD
GPIO27	GPIO27	0	0
GPIO28	GPIO28	0	0
GPIO29	GPIO29	0	0
GPIO30	GPIO30	0	0
GPIO31	GPIO31	0	0
GPIO32	GPIO32	0	0
GPIO33	GPIO33	0	0
GPIO34	GPIO34	0	1
GPIO35	GPIO35	0	0
GPIO36	GPIO36	1	0
GPIO37	GPIO37	1	0
GPIO38	GPIO38	1	0
GPIO39	GPIO39	1	0
GPIO40	GPIO40	1	0
GPIO41	GPIO41	1	0
GPIO42	GPIO42	1	0
GPIO43	GPIO43	1	0
GPIO44	GPIO44	1	0
GPIO45	GPIO45	1	0
GPIO46	GPIO46	1	0
GPIO47	GPIO47	1	0
GPIO48	GPIO48	1	0
GPIO49	GPIO49	0	0
GPIO50	GPIO50	0	0
GPIO51	GPIO51	0	0
GPIO52	GPIO52	1	0
GPIO53	GPIO53	0	0
GPIO54	GPIO54	0	0
GPIO55	GPIO55	0	0
GPIO56	GPIO56	1	0
GPIO57	GPIO57	0	0
GPIO58	GPIO58	0	0
GPIO59	GPIO59	0	0
GPIO60	GPIO60	1	0

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Table 2-13 System Signal Description (continued)

Signal Name	Description	PU	PD
GPIO61	GPIO61	0	0
GPIO62	GPIO62	0	0
GPIO63	GPIO63	0	0
RSTN	Reset Negative	Tied to 1	Tied to 0
RTC_XIN	RTC Input Signal	NONE	NONE
RTC_XOUT	RTC Output Signal	NONE	NONE
OSC_XIN	Oscillator Input Signal	NONE	NONE
OSC_XOUT	Oscillator Output Signal	NONE	NONE
SD0_CLK	SD0 Clock Signal	0	0
SD0_CMD	SD0 Command Signal	0	0
SD0_DATA0	SD0 DATA Lane 0	1	0
SD0_DATA1	SD0 DATA Lane 1	0	0
SD0_DATA2	SD0 DATA Lane 2	0	0
SD0_DATA3	SD0 DATA Lane 3	1	0
SD0_DATA4	SD0 DATA Lane 4	1	0
SD0_DATA5	SD0 DATA Lane 5	0	0
SD0_DATA6	SD0 DATA Lane 6	0	0
SD0_DATA7	SD0 DATA Lane 7	0	0
SD0_STRB	SD0 STR8	0	0
GMAC1_MDC	GMAC1 Management Device Clock	NONE	NONE
GMAC1_MDIO	GMAC1 Management Data Input and Output	NONE	NONE
GMAC1_RXD0	GMAC1 Input Data Lane 0	NONE	NONE
GMAC1_RXD1	GMAC1 Input Data Lane 1	NONE	NONE
GMAC1_RXD2	GMAC1 Input Data Lane 2	NONE	NONE
GMAC1_RXD3	GMAC1 Input Data Lane 3	NONE	NONE
GMAC1_RXDV	GMAC1 Input Collision and Data Valid	NONE	NONE
GMAC1_RXC	GMAC1 Input Clock	NONE	NONE
GMAC1_TXD0	GMAC1 Output Data Lane 0	NONE	NONE
GMAC1_TXD1	GMAC1 Output Data Lane 1	NONE	NONE
GMAC1_TXD2	GMAC1 Output Data Lane 2	NONE	NONE
GMAC1_TXD3	GMAC1 Output Data Lane 3	NONE	NONE
GMAC1_TXEN	GMAC1 Output Enable	NONE	NONE
GMAC1_TXC	GMAC1 Output Clock	NONE	NONE
GMAC0_MDC	GMAC0 Management Device Clock	NONE	NONE

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Table 2-13 System Signal Description (continued)

Signal Name	Description	PU	PD
GMAC0_MDIO	GMAC0 Management Data Input and Output	NONE	NONE
GMAC0_RXD0	GMAC0 Input Data Lane 0	NONE	NONE
GMAC0_RXD1	GMAC0 Input Data Lane 1	NONE	NONE
GMAC0_RXD2	GMAC0 Input Data Lane 2	NONE	NONE
GMAC0_RXD3	GMAC0 Input Data Lane 3	NONE	NONE
GMAC0_RXDV	GMAC0 Input Collision and Data Valid	NONE	NONE
GMAC0_RXC	GMAC0 Input Clock	NONE	NONE
GMAC0_TXD0	GMAC0 Output Data Lane 0	NONE	NONE
GMAC0_TXD1	GMAC0 Output Data Lane 1	NONE	NONE
GMAC0_TXD2	GMAC0 Output Data Lane 2	NONE	NONE
GMAC0_TXD3	GMAC0 Output Data Lane 3	NONE	NONE
GMAC0_TXEN	GMAC0 Output Enable	NONE	NONE
GMAC0_TXC	GMAC0 Output Clock	NONE	NONE
QSPI_SCLK	QSPI_SCLK	0	0
QSPI_CSn0	QSPI Chip Select	1	0
QSPI_DATA0	QSPI Data Lane 0	0	0
QSPI_DATA1	QSPI Data Lane 1	0	0
QSPI_DATA2	QSPI Data Lane 2	0	0
QSPI_DATA3	QSPI Data lane 3	0	0
OTP_PENVDD2	OTP_PENVDD2	NONE	NONE
DDR_ACT_N	DDR_ACT_N	NONE	NONE
DDR_ADR[13:0]	DDR Address [13:0]	NONE	NONE
DDR_ATB0	DDR_ATB0	NONE	NONE
DDR_ATB1	DDR_ATB1	NONE	NONE
DDR_BA[1:0]	DDR BANK Address Input [1:0]	NONE	NONE
DDR_BG[1:0]	DDR_BG[1:0]	NONE	NONE
DDR_CAL	DDR_CAL	NONE	NONE
DDR_CAS_N_ADR15	DDR Column Address Select Address 15	NONE	NONE
DDR_CKE[1:0]	DDR Clock Enable [1:0]	NONE	NONE
DDR_CK_N[1:0]	DDR Clock Negative [1:0]	NONE	NONE
DDR_CK_P[1:0]	DDR Clock Positive [1:0]	NONE	NONE
DDR_CS_N[3:0]	DDR Chip Select Negative [3:0]	NONE	NONE
DDR_DM_DBI_N[3:0]	DDR_DM_DBI_N[3:0]	NONE	NONE
DDR_DQ[0:31]	DDR Data Communication [0:31]	NONE	NONE

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Table 2-13 System Signal Description (continued)

Signal Name	Description	PU	PD
DDR_DQS_N[3:0]	DDR Data Communication Select Negative [3:0]	NONE	NONE
DDR_DQS_P[3:0]	DDR Data Communication Select Positive [3:0]	NONE	NONE
DDR_ERR_N	DDR Error Negative	NONE	NONE
DDR_ODT[1:0]	DDR On-Die Termination [1:0]	NONE	NONE
DDR_PAR	DDR_PAR	NONE	NONE
DDR_PLL_REFOUT_N	DDR PLL Reference Output Negative	NONE	NONE
DDR_PLL_REFOUT_P	DDR PLL Reference Output Positive	NONE	NONE
DDR_PLL_TESTOUT_N	DDR PLL Test Output Negative	NONE	NONE
DDR_PLL_TESTOUT_P	DDR PLL Test Output Positive	NONE	NONE
DDR_RAS_N_ADR16	DDR Row Address Select Negative Address 16	NONE	NONE
DDR_RESET_N	DDR Reset Negative	NONE	NONE
DDR_WE_N_ADR14	DDR Write Enable Negative Address 14	NONE	NONE
HDMITX0_EXTR	HDMI Output 0 Extra	NONE	NONE
HDMITX0_TX0N	HDMI Output 0 Negative	NONE	NONE
HDMITX0_TX0P	HDMI Output 0 Positive	NONE	NONE
HDMITX0_TX1N	HDMI Output 1 Negative	NONE	NONE
HDMITX0_TX1P	HDMI Output 1 Positive	NONE	NONE
HDMITX0_TX2N	HDMI Output 2 Negative	NONE	NONE
HDMITX0_TX2P	HDMI Output 2 Positive	NONE	NONE
HDMITX0_TX3N	HDMI Output 3 Negative	NONE	NONE
HDMITX0_TX3P	HDMI Output 3 Positive	NONE	NONE
MIPITX_L0N	MIPI Output Lane 0 Negative	NONE	NONE
MIPITX_L0P	MIPI Output Lane 0 Positive	NONE	NONE
MIPITX_L1N	MIPI Output Lane 1 Negative	NONE	NONE
MIPITX_L1P	MIPI Output Lane 1 Positive	NONE	NONE
MIPITX_L2N	MIPI Output Lane 2 Negative	NONE	NONE
MIPITX_L2P	MIPI Output Lane 2 Positive	NONE	NONE
MIPITX_L3N	MIPI Output Lane 3 Negative	NONE	NONE
MIPITX_L3P	MIPI Output Lane 3 Positive	NONE	NONE
MIPITX_L4N	MIPI Output Lane 4 Negative	NONE	NONE
MIPITX_L4P	MIPI Output Lane 4 Positive	NONE	NONE
MIPIRX_DN0	MIPI Input DN Lane 0	NONE	NONE
MIPIRX_DN1	MIPI Input DN Lane 1	NONE	NONE
MIPIRX_DN2	MIPI Input DN Lane 2	NONE	NONE

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Table 2-13 System Signal Description (continued)

Signal Name	Description	PU	PD
MIPIRX_DN3	MIPI Input DN Lane 3	NONE	NONE
MIPIRX_DN4	MIPI Input DN Lane 4	NONE	NONE
MIPIRX_DN5	MIPI Input DN Lane 5	NONE	NONE
MIPIRX_DP0	MIPI Input DP Lane 0	NONE	NONE
MIPIRX_DP1	MIPI Input DP Lane 1	NONE	NONE
MIPIRX_DP2	MIPI Input DP Lane 2	NONE	NONE
MIPIRX_DP3	MIPI Input DP Lane 3	NONE	NONE
MIPIRX_DP4	MIPI Input DP Lane 4	NONE	NONE
MIPIRX_DP5	MIPI Input DP Lane 5	NONE	NONE
PCIE0_CKREFN	PCIE0 Clock Reference Negative	NONE	NONE
PCIE0_CKREFP	PCIE0 Clock Reference Positive	NONE	NONE
PCIE0_RXN	PCIE0 Input Negative	NONE	NONE
PCIE0_RXP	PCIE0 Input Positive	NONE	NONE
PCIE0_TXN	PCIE0 Output Negative	NONE	NONE
PCIE0_TXP	PCIE0 Output Positive	NONE	NONE
PCIE1_CKREFN	PCIE1 Clock Reference Negative	NONE	NONE
PCIE1_CKREFP	PCIE1 Clock Reference Positive	NONE	NONE
PCIE1_RXN	PCIE1 Input Negative	NONE	NONE
PCIE1_RXP	PCIE1 Input Positive	NONE	NONE
PCIE1_TXN	PCIE1 Output Negative	NONE	NONE
PCIE1_TXP	PCIE1 Output Positive	NONE	NONE
USB_DM	USB Device Management	NONE	NONE
USB_DP	USB DP	NONE	NONE
USB_ID	USB ID	NONE	NONE
USB_RREF	USB_RREF	NONE	NONE
USB_VBUS	USB_VBUS	NONE	NONE
ANA18_TEMP_VCAL	Analog 18 Temperature VCAL	NONE	NONE
ANA18_TEMP_VSS	Analog 18 Temperature VSS	NONE	NONE
ANA18_TEMP_TEST1	Analog 18 Temperature Test 1	NONE	NONE
ANA18_TEMP_TEST0	Analog 18 Temperature Test 0	NONE	NONE

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2.6.1. Pin Map

The following figure provides a general view of the pins and their corresponding signal names, for more detailed information, see Pin List *(on page 70)*.

In the figure, a letter on the left edge from “A” to “AE” and a number on the top edge from “1” to “25” are used together to indicate a pin location. For example, A1 = “VSS”, A2 = “QSPI_DATA0”, and so forth.

Figure 2-6 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	VSS	QSPI_DATA0	QSPI_SCLK	GPIO0	AVSS_PCIE1	PCIE1_CKREFN	AVSS_PCIE1	PCIE1_TXP	AVSS_PCIE0	PCIE0_CKREFN	AVSS_PCIE0	PCIE0_TXP	AVSS_PCIE0	USB_ID	USB_DP	USB_DM	GPIO49	GPIO53	GPIO51	AVSS_HDMI	HDMITX0_TX2P	HDMITX0_TX2N	HDMITX0_TX1P	HDMITX0_TX1N	AVSS_HDMI
B	QSPI_DATA2	QSPI_DATA1	QSPI_CSN0	GPIO2	AVSS_PCIE1	PCIE1_CKREFP	AVSS_PCIE1	PCIE1_TXN	AVSS_PCIE1	PCIE0_CKREFP	AVSS_PCIE0	PCIE0_TXN	AVSS_PCIE0	USB_VBUS18	VCCA33_USB	AVSS_USB	VSS	GPIO52	GPIO41	GPIO42	AVSS_HDMI	AVSS_HDMI	AVSS_HDMI	AVSS_HDMI	AVSS_HDMI
C	QSPI_DATA3	VSS	PAD_QSPI_SEL18	GPIO1	GPIO3	GPIO4	PCIE1_RXP	AVSS_PCIE1	AVDL_PCIE1	AVSS_PCIE0	PCIE0_RXP	AVDL_PCIE0	AVSS_PCIE0	USB_RREF	VCCA18_USB	AVSS_USB	GPIO45	VSS	GPIO39	VSS	GPIO59	AVDD09_HDMI	AVDD_HDMI	HDMITX0_TX0P	HDMITX0_TX0N
D	SD0_DATA0	SD0_CLK	VDD1833_QSPI	VSS	GPIO6	GPIO5	PCIE1_RXN	AVSS_PCIE1	AVDH_PCIE1	AVSS_PCIE0	PCIE0_RXN	AVSS_PCIE0	AVSS_PCIE0	AVDD09_USB	GPIO50	GPIO56	GPIO62	GPIO37	VSS	GPIO63	GPIO36	AVDD_HDMI	AVSS_HDMI	AVSS_HDMI	HDMITX0_TX3P
E	SD0_DATA1	SD0_DATA3	VSS	SD0_CMD	SD0_DATA2	PAD_SD_SEL18	VSS	VDD1833_GPIO3	VSS	VSS	AVSS_PCIE0	VSS	AVDH_PCIE0	AVSS_USB	GPIO54	GPIO48	VSS	GPIO46	GPIO55	VSS	GPIO43	PVSS_HDMI	PVDD_HDMI	HDMITX0_EXTR	HDMITX0_TX3N
F	GPIO18	GPIO16	SD0_DATA4	SD0_DATA5	SD0_DATA7	SD0_DATA6	SD0_STRB	VSS	VDD1833_SD0	VSS	VSS	VSS	VSS	GPIO47	VDD1833_GPIO2	VDD1833_GPIO2	GPIO38	GPIO40	GPIO60	GPIO61	GPIO57	GPIO44	VSS	VSS	AVSS_HDMI
G	GPIO17	VSS	GPIO15	GPIO14	GPIO20	GPIO19	VSS	VSS	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	GPIO58	VSS	VSS	MIPITX_L0N	MIPITX_L0P
H	GPIO9	GPIO11	GPIO13	VSS	GPIO12	VDD1833_GPIO4	VSS	VDD	VDD	VSS	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	MIPITX_L1N	MIPITX_L1P
J	GPIO8	VSS	GPIO7	GPIO10	VSS	VDD	VDD	VSS	VSS	VSS	VDD_CPU	VDD_CPU	VDD_CPU	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VDD	VSS	VSS	MIPITX_L2N	MIPITX_L2P
K	GMAC1_TXD3	GMAC1_TXC	GMAC1_RXDV	GMAC1_TXD2	GMAC1_TXEN	VSS	VDD	VSS	VSS	VDD_CPU	VSS	VDD_CPU	VDD_CPU	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VDD	VSS	VDD_MIPITX	MIPITX_L3N	MIPITX_L3P
L	GMAC1_TXD0	VSS	GMAC1_RXD0	VSS	VSS	VSS	VDD	VDD	VSS	VDD_CPU	VSS	VDD_CPU	VDD_CPU	VSS	VSS	VDD	VDD	VDD	VSS	VDD	VSS	VCC18A_MIPITX	VSS	MIPITX_L4N	MIPITX_L4P
M	GMAC1_RXD1	GMAC1_MDIO	GMAC1_RXC	GMAC1_TXD1	VDD1825_GMAC1	VSS	VSS	VDD	VSS	VDD_CPU	VDD_CPU	VDD_CPU	VDD_CPU	VSS	VSS	VSS	VSS	VDD	VSS	VSS	VSS	VSS	GND09A_MIPIRX	MIPIRX_DN5	MIPIRX_DP5
N	GMAC1_MDC	GMAC1_RXD3	GMAC1_RXD2	VDD1825_GMAC0	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS	VSS	VCC18A_MIPIRX	GND09A_MIPIRX	MIPIRX_DN4	MIPIRX_DP4
P	GMAC0_TXEN	VSS	GMAC0_TXD2	VSS	OTP_PENVDD2	VSS18_OTP	VDD18_OTP	VSS	VDD	VDD	VDD	VDD	VSS	VDD	VDD	VSS	VDD	VSS	VDDA18_TEMP	VSS	VSS	VCC09A_MIPIRX	GND09A_MIPIRX	MIPIRX_DN3	MIPIRX_DP3
R	GMAC0_TXD1	GMAC0_TXC	VSS	GMAC0_RXD1	VCCA18_PLL0	VCCA18_PLL2	VCCA18_PLL1	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS18_TEMP	ANA18_TEMP_VSS	ANA18_TEMP_TEST1	GND09A_MIPIRX	GND09A_MIPIRX	MIPIRX_DN2	MIPIRX_DP2
T	GMAC0_RXDV	GMAC0_RXC	GMAC0_TXD3	VSS	VSS_PLL0	VSS_PLL2	VSS_PLL1	VSS	VDD_DDR	VDD_DDR	VSS	VDDQ_DDR	VDDQ_DDR	VDDPLL_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VSS	VDD18_TEMP	ANA18_TEMP_VCAL	ANA18_TEMP_TEST0	GPIO35	GND09A_MIPIRX	MIPIRX_DN1	MIPIRX_DP1
U	VSS	GMAC0_RXD2	GMAC0_RXD0	GMAC0_TXD0	VDD_PLL0	VDD_PLL2	VDD_PLL1	VSS	VDD_DDR	VDD_DDR	VSS	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VSS	VSS	VDD1833_GPIO1	GPIO34	GPIO33	GND09A_MIPIRX	MIPIRX_DN0	MIPIRX_DP0
V	RSTN	GMAC0_MDC	GMAC0_RXD3	GMAC0_MDIO	VSS_PLL0	VSS_PLL2	VSS_PLL1	VSS	VDD_DDR	VDD_DDR	VSS	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VDDQ_DDR	VSS	VSS	VDD1833_GPIO1	VSS	GPIO32	VSS	GPIO28	GND09A_MIPIRX	GND09A_MIPIRX
W	TESTEN	RGPIO2	VSS	RGPIO0	RGPIO1	RGPIO3	VSS	VDD_DDR	VDD_DDR	VSS	VSS	VSS	VSS	VDDQCK_DDR	VSS	VSS	VSS	VSS	GPIO29	GPIO31	GPIO27	GPIO24	GPIO26	GPIO21	GPIO25
Y	RTC_XIN	RTC_XOUT	VDD_RTC	VSS	VDD1833_AON	VSS	VDD_DDR	VDD_DDR	VSS	VSS	VSS	DDR_ADR[5]	DDR_BG[1]	VSS	DDR_PLL_REFOUT_N	DDR_CKE[1]	DDR_PLL_TESTOUT_P	VSS	VSS	GPIO30	GPIO22	VSS	GPIO23	VSS	DDR_DQ[3]
AA	VSS_RTC	VSS18_OSC	VDD18_OSC	VSS	VSS	VSS	VDD_DDR	VSS	VSS	DDR_ADR[13]	DDR_ADR[6]	DDR_ADR[7]	DDR_BA[1]	DDR_CS_N[3]	DDR_PLL_REFOUT_P	VSS	DDR_PLL_TESTOUT_N	DDR_CKE[0]	VSS	VSS	DDR_DQ[9]	DDR_DQ[13]	DDR_DQ[7]	DDR_DQ[6]	DDR_DM_DBI_N[0]
AB	OSC_XIN	OSC_XOUT	VSS	DDR_DQ[28]	DDR_DQ[31]	VSS	VSS	DDR_DQ[23]	DDR_DQ[20]	VSS	DDR_ADR[0]	DDR_ACT_N	VSS	DDR_RAS_N_ADR16	DDR_CAS_N_ADR15	DDR_BA[0]	DDR_CS_N[1]	DDR_RESET_N	VSS	DDR_DQ[12]	DDR_DQ[11]	VSS	DDR_DQ[2]	VSS	DDR_DQ[0]
AC	VSS	VSS	DDR_DQ[29]	VSS	DDR_DQ[30]	VSS	DDR_DQ[22]	VSS	DDR_DQ[18]	DDR_ADR[12]	DDR_ADR[11]	DDR_ADR[8]	DDR_ADR[2]	DDR_ADR[1]	DDR_BG[0]	DDR_ATB1	VSS	DDR_CS_N[0]	DDR_ODT[0]	DDR_DQ[15]	VSS	DDR_DQ[10]	VSS	DDR_DQ[4]	DDR_DQ[1]
AD	DDR_DM_DBI_N[3]	DDR_DQ[27]	DDR_DQ[25]	DDR_DQS_N[3]	VSS	DDR_DQ[21]	DDR_DQS_N[2]	DDR_DQ[19]	DDR_DQ[17]	VSS	DDR_ADR[10]	DDR_CK_P[1]	DDR_ADR[3]	VSS	DDR_CK_N[0]	DDR_ERR_N	DDR_ATB0	DDR_CS_N[2]	DDR_ODT[1]	DDR_DQ[14]	DDR_DQ[8]	DDR_DQS_P[1]	DDR_DQ[5]	DDR_DQS_N[0]	VSS
AE	VSS	VSS	DDR_DQ[24]	DDR_DQS_P[3]	DDR_DQ[26]	DDR_DM_DBI_N[2]	DDR_DQS_P[2]	VSS	DDR_DQ[16]	DDR_ADR[9]	DDR_ADR[4]	DDR_CK_N[1]	VSS	DDR_PAR	DDR_CK_P[0]	VSS	DDR_WE_N_ADR1	VSS	DDR_CAL	DDR_DM_DBI_N[1]	VSS	DDR_DQS_N[1]	VSS	DDR_DQS_P[0]	VSS

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2.6.2. Pin List

The following table shows the signal names for each pin.

Table 2-14 Pin List Description (A)

Pin No.	Signal Name
A1	VSS
A2	QSPI_DATA0
A3	QSPI_SCLK
A4	GPIO0
A5	AVSS_PCIE1
A6	PCIE1_CKREFN
A7	AVSS_PCIE1
A8	PCIE1_TXP
A9	AVSS_PCIE0
A10	PCIE0_CKREFN
A11	AVSS_PCIE0
A12	PCIE0_TXP
A13	AVSS_PCIE0
A14	USB_ID
A15	USB_DP
A16	USB_DM
A17	GPIO49
A18	GPIO53
A19	GPIO51
A20	AVSS_HDMI
A21	HDMITX0_TX2P
A22	HDMITX0_TX2N
A23	HDMITX0_TX1P
A24	HDMITX0_TX1N
A25	AVSS_HDMI

Table 2-15 Pin List Description (B)

Pin No.	Signal Name
B1	QSPI_DATA2
B2	QSPI_DATA1
B3	QSPI_CSN0
B4	GPIO2
B5	AVSS_PCIE1
B6	PCIE1_CKREFP
B7	AVSS_PCIE1
B8	PCIE1_TXN
B9	AVSS_PCIE1
B10	PCIE0_CKREFP
B11	AVSS_PCIE0
B12	PCIE0_TXN
B13	AVSS_PCIE0
B14	USB_VBUS18
B15	VCCA33_USB
B16	AVSS_USB
B17	VSS
B18	GPIO52
B19	GPIO41
B20	GPIO42
B21	AVSS_HDMI
B22	AVSS_HDMI
B23	AVSS_HDMI
B24	AVSS_HDMI
B25	AVSS_HDMI

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Table 2-16 Pin List Description (C)

Pin No.	Signal Name
C1	QSPI_DATA3
C2	VSS
C3	QSPI_SEL18
C4	GPIO1
C5	GPIO3
C6	GPIO4
C7	PCIE1_RXP
C8	AVSS_PCIE1
C9	AVDL_PCIE1
C10	AVSS_PCIE0
C11	PCIE0_RXP
C12	AVDL_PCIE0
C13	AVSS_PCIE0
C14	USB_RREF
C15	VCCA18_USB
C16	AVSS_USB
C17	GPIO45
C18	VSS
C19	GPIO39
C20	VSS
C21	GPIO59
C22	AVDD09_HDMI
C23	AVDD_HDMI
C24	HDMITX0_TX0P
C25	HDMITX0_TX0N

Table 2-17 Pin List Description (D)

Pin No.	Signal Name
D1	SD0_DATA0
D2	SD0_CLK
D3	VDD1833_QSPI
D4	VSS
D5	GPIO6
D6	GPIO5
D7	PCIE1_RXN
D8	AVSS_PCIE1
D9	AVDH_PCIE1
D10	AVSS_PCIE0
D11	PCIE0_RXN
D12	AVSS_PCIE0
D13	AVSS_PCIE0
D14	AVDD09_USB
D15	GPIO50
D16	GPIO56
D17	GPIO62
D18	GPIO37
D19	VSS
D20	GPIO63
D21	GPIO36
D22	AVDD_HDMI
D23	AVSS_HDMI
D24	AVSS_HDMI
D25	HDMITX0_TX3P

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Table 2-18 Pin List Description (E)

Pin No.	Signal Name
E1	SD0_DATA1
E2	SD0_DATA3
E3	VSS
E4	SD0_CMD
E5	SD0_DATA2
E6	SD_SEL18
E7	VSS
E8	VDD1833_GPIO3
E9	VSS
E10	VSS
E11	AVSS_PCIE0
E12	VSS
E13	AVDH_PCIE0
E14	AVSS_USB
E15	GPIO54
E16	GPIO48
E17	VSS
E18	GPIO46
E19	GPIO55
E20	VSS
E21	GPIO43
E22	PVSS_HDMI
E23	PVDD_HDMI
E24	HDMITX0_EXTR
E25	HDMITX0_TX3N

Table 2-19 Pin List Description (F)

Pin No.	Signal Name
F1	GPIO18
F2	GPIO16
F3	SD0_DATA4
F4	SD0_DATA5
F5	SD0_DATA7
F6	SD0_DATA6
F7	SD0_STRB
F8	VSS
F9	VDD1833_SD0
F10	VSS
F11	VSS
F12	VSS
F13	VSS
F14	GPIO47
F15	VDD1833_GPIO2
F16	VDD1833_GPIO2
F17	GPIO38
F18	GPIO40
F19	GPIO60
F20	GPIO61
F21	GPIO57
F22	GPIO44
F23	VSS
F24	VSS
F25	AVSS_HDMI

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Table 2-20 Pin List Description (G)

Pin No.	Signal Name
G1	GPIO17
G2	VSS
G3	GPIO15
G4	GPIO14
G5	GPIO20
G6	GPIO19
G7	VSS
G8	VSS
G9	VDD
G10	VDD
G11	VDD
G12	VSS
G13	VSS
G14	VSS
G15	VSS
G16	VSS
G17	VSS
G18	VSS
G19	VSS
G20	VSS
G21	GPIO58
G22	VSS
G23	VSS
G24	MIPITX_L0N
G25	MIPITX_L0P

Table 2-21 Pin List Description (H)

Pin No.	Signal Name
H1	GPIO9
H2	GPIO11
H3	GPIO13
H4	VSS
H5	GPIO12
H6	VDD1833_GPIO4
H7	VSS
H8	VDD
H9	VDD
H10	VSS
H11	VDD
H12	VSS
H13	VSS
H14	VSS
H15	VSS
H16	VDD
H17	VDD
H18	VDD
H19	VDD
H20	VDD
H21	VSS
H22	VSS
H23	VSS
H24	MIPITX_L1N
H25	MIPITX_L1P

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Table 2-22 Pin List Description (J)

Pin No.	Signal Name
J1	GPIO8
J2	VSS
J3	GPIO7
J4	GPIO10
J5	VSS
J6	VDD
J7	VDD
J8	VSS
J9	VSS
J10	VSS
J11	VDD_CPU
J12	VDD_CPU
J13	VDD_CPU
J14	VSS
J15	VSS
J16	VDD
J17	VSS
J18	VDD
J19	VSS
J20	VDD
J21	VDD
J22	VSS
J23	VSS
J24	MIPITX_L2N
J25	MIPITX_L2P

Table 2-23 Pin List Description (K)

Pin No.	Signal Name
K1	GMAC1_TXD3
K2	GMAC1_TXC
K3	GMAC1_RXDV
K4	GMAC1_TXD2
K5	GMAC1_TXEN
K6	VSS
K7	VDD
K8	VSS
K9	VSS
K10	VDD_CPU
K11	VSS
K12	VDD_CPU
K13	VDD_CPU
K14	VSS
K15	VSS
K16	VDD
K17	VSS
K18	VDD
K19	VSS
K20	VDD
K21	VDD
K22	VSS
K23	VDD_MIPITX
K24	MIPITX_L3N
K25	MIPITX_L3P

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Table 2-24 Pin List Description (L)

Pin No.	Signal Name
L1	GMAC1_TXD0
L2	VSS
L3	GMAC1_RXD0
L4	VSS
L5	VSS
L6	VSS
L7	VDD
L8	VDD
L9	VSS
L10	VDD_CPU
L11	VSS
L12	VDD_CPU
L13	VDD_CPU
L14	VSS
L15	VSS
L16	VDD
L17	VDD
L18	VDD
L19	VSS
L20	VDD
L21	VSS
L22	VCC18A_MIPITX
L23	VSS
L24	MIPITX_L4N
L25	MIPITX_L4P

Table 2-25 Pin List Description (M)

Pin No.	Signal Name
M1	GMAC1_RXD1
M2	GMAC1_MDIO
M3	GMAC1_RXC
M4	GMAC1_TXD1
M5	VDD1825_GMAC1
M6	VSS
M7	VSS
M8	VDD
M9	VSS
M10	VDD_CPU
M11	VDD_CPU
M12	VDD_CPU
M13	VDD_CPU
M14	VSS
M15	VSS
M16	VSS
M17	VSS
M18	VDD
M19	VSS
M20	VSS
M21	VSS
M22	VSS
M23	GND09A_MIPIRX
M24	MIPIRX_DN5
M25	MIPIRX_DP5

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Table 2-26 Pin List Description (N)

Pin No.	Signal Name
N1	GMAC1_MDC
N2	GMAC1_RXD3
N3	GMAC1_RXD2
N4	VDD1825_GMAC0
N5	VSS
N6	VSS
N7	VSS
N8	VDD
N9	VDD
N10	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VDD
N15	VDD
N16	VDD
N17	VDD
N18	VDD
N19	VSS
N20	VSS
N21	VSS
N22	VCC18A_MIPIRX
N23	GND09A_MIPIRX
N24	MIPIRX_DN4
N25	MIPIRX_DP4

Table 2-27 Pin List Description (P)

Pin No.	Signal Name
P1	GMAC0_TXEN
P2	VSS
P3	GMAC0_TXD2
P4	VSS
P5	OTP_PENVDD2
P6	VSS18_OTP
P7	VDD18_OTP
P8	VSS
P9	VDD
P10	VDD
P11	VDD
P12	VDD
P13	VSS
P14	VDD
P15	VDD
P16	VSS
P17	VDD
P18	VSS
P19	VDDA18_TEMP
P20	VSS
P21	VSS
P22	VCC09A_MIPIRX
P23	GND09A_MIPIRX
P24	MIPIRX_DN3
P25	MIPIRX_DP3

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Table 2-28 Pin List Description (R)

Pin No.	Signal Name
R1	GMAC0_TXD1
R2	GMAC0_TXC
R3	VSS
R4	GMAC0_RXD1
R5	VCCA18_PLL0
R6	VCCA18_PLL2
R7	VCCA18_PLL1
R8	VSS
R9	VDD
R10	VSS
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS
R16	VSS
R17	VSS
R18	VSS
R19	VSS18_TEMP
R20	ANA18_TEMP_VSS
R21	ANA18_TEMP_TEST1
R22	GND09A_MIPIRX
R23	GND09A_MIPIRX
R24	MIPIRX_DN2
R25	MIPIRX_DP2

Table 2-29 Pin List Description (T)

Pin No.	Signal Name
T1	GMAC0_RXDV
T2	GMAC0_RXC
T3	GMAC0_TXD3
T4	VSS
T5	VSS_PLL0
T6	VSS_PLL2
T7	VSS_PLL1
T8	VSS
T9	VDD_DDR
T10	VDD_DDR
T11	VSS
T12	VDDQ_DDR
T13	VDDQ_DDR
T14	VDDPLL_DDR
T15	VDDQ_DDR
T16	VDDQ_DDR
T17	VDDQ_DDR
T18	VSS
T19	VDD18_TEMP
T20	ANA18_TEMP_VCAL
T21	ANA18_TEMP_TEST0
T22	GPIO35
T23	GND09A_MIPIRX
T24	MIPIRX_DN1
T25	MIPIRX_DP1

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Table 2-30 Pin List Description (U)

Pin No.	Signal Name
U1	VSS
U2	GMAC0_RXD2
U3	GMAC0_RXD0
U4	GMAC0_TXD0
U5	VDD_PLL0
U6	VDD_PLL2
U7	VDD_PLL1
U8	VSS
U9	VDD_DDR
U10	VDD_DDR
U11	VSS
U12	VDDQ_DDR
U13	VDDQ_DDR
U14	VDDQ_DDR
U15	VDDQ_DDR
U16	VDDQ_DDR
U17	VDDQ_DDR
U18	VSS
U19	VSS
U20	VDD1833_GPIO1
U21	GPIO34
U22	GPIO33
U23	GND09A_MIPIRX
U24	MIPIRX_DN0
U25	MIPIRX_DP0

Table 2-31 Pin List Description (V)

Pin No.	Signal Name
V1	RSTN
V2	GMAC0_MDC
V3	GMAC0_RXD3
V4	GMAC0_MDIO
V5	VSS_PLL0
V6	VSS_PLL2
V7	VSS_PLL1
V8	VSS
V9	VDD_DDR
V10	VDD_DDR
V11	VSS
V12	VDDQ_DDR
V13	VDDQ_DDR
V14	VDDQ_DDR
V15	VDDQ_DDR
V16	VDDQ_DDR
V17	VSS
V18	VSS
V19	VDD1833_GPIO1
V20	VSS
V21	GPIO32
V22	VSS
V23	GPIO28
V24	GND09A_MIPIRX
V25	GND09A_MIPIRX

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Table 2-32 Pin List Description (W)

Pin No.	Signal Name
W1	TESTEN
W2	RGPIO2
W3	VSS
W4	RGPIO0
W5	RGPIO1
W6	RGPIO3
W7	VSS
W8	VDD_DDR
W9	VDD_DDR
W10	VSS
W11	VSS
W12	VSS
W13	VSS
W14	VDDQCK_DDR
W15	VSS
W16	VSS
W17	VSS
W18	VSS
W19	GPIO29
W20	GPIO31
W21	GPIO27
W22	GPIO24
W23	GPIO26
W24	GPIO21
W25	GPIO25

Table 2-33 Pin List Description (Y)

Pin No.	Signal Name
Y1	RTC_XIN
Y2	RTC_XOUT
Y3	VDD_RTC
Y4	VSS
Y5	VDD1833_AON
Y6	VSS
Y7	VDD_DDR
Y8	VDD_DDR
Y9	VSS
Y10	VSS
Y11	VSS
Y12	DDR_ADR[5]
Y13	DDR_BG[1]
Y14	VSS
Y15	DDR_PLL_REFOUT_N
Y16	DDR_CKE[1]
Y17	DDR_PLL_TESTOUT_P
Y18	VSS
Y19	VSS
Y20	GPIO30
Y21	GPIO22
Y22	VSS
Y23	GPIO23
Y24	VSS
Y25	DDR_DQ[3]

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Table 2-34 Pin List Description (AA)

Pin No.	Signal Name
AA1	VSS_RTC
AA2	VSS18_OSC
AA3	VDD18_OSC
AA4	VSS
AA5	VSS
AA6	VSS
AA7	VDD_DDR
AA8	VSS
AA9	VSS
AA10	DDR_ADR[13]
AA11	DDR_ADR[6]
AA12	DDR_ADR[7]
AA13	DDR_BA[1]
AA14	DDR_CS_N[3]
AA15	DDR_PLL_REFOUT_P
AA16	VSS
AA17	DDR_PLL_TESTOUT_N
AA18	DDR_CKE[0]
AA19	VSS
AA20	VSS
AA21	DDR_DQ[9]
AA22	DDR_DQ[13]
AA23	DDR_DQ[7]
AA24	DDR_DQ[6]
AA25	DDR_DM_DBI_N[0]

Table 2-35 Pin List Description (AB)

Pin No.	Signal Name
AB1	OSC_XIN
AB2	OSC_XOUT
AB3	VSS
AB4	DDR_DQ[28]
AB5	DDR_DQ[31]
AB6	VSS
AB7	VSS
AB8	DDR_DQ[23]
AB9	DDR_DQ[20]
AB10	VSS
AB11	DDR_ADR[0]
AB12	DDR_ACT_N
AB13	VSS
AB14	DDR_RAS_N_ADR16
AB15	DDR_CAS_N_ADR15
AB16	DDR_BA[0]
AB17	DDR_CS_N[1]
AB18	DDR_RESET_N
AB19	VSS
AB20	DDR_DQ[12]
AB21	DDR_DQ[11]
AB22	VSS
AB23	DDR_DQ[2]
AB24	VSS
AB25	DDR_DQ[0]

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Table 2-36 Pin List Description (AC)

Pin No.	Signal Name
AC1	VSS
AC2	VSS
AC3	DDR_DQ[29]
AC4	VSS
AC5	DDR_DQ[30]
AC6	VSS
AC7	DDR_DQ[22]
AC8	VSS
AC9	DDR_DQ[18]
AC10	DDR_ADR[12]
AC11	DDR_ADR[11]
AC12	DDR_ADR[8]
AC13	DDR_ADR[2]
AC14	DDR_ADR[1]
AC15	DDR_BG[0]
AC16	DDR_ATB1
AC17	VSS
AC18	DDR_CS_N[0]
AC19	DDR_ODT[0]
AC20	DDR_DQ[15]
AC21	VSS
AC22	DDR_DQ[10]
AC23	VSS
AC24	DDR_DQ[4]
AC25	DDR_DQ[1]

Table 2-37 Pin List Description (AD)

Pin No.	Signal Name
AD1	DDR_DM_DBI_N[3]
AD2	DDR_DQ[27]
AD3	DDR_DQ[25]
AD4	DDR_DQS_N[3]
AD5	VSS
AD6	DDR_DQ[21]
AD7	DDR_DQS_N[2]
AD8	DDR_DQ[19]
AD9	DDR_DQ[17]
AD10	VSS
AD11	DDR_ADR[10]
AD12	DDR_CK_P[1]
AD13	DDR_ADR[3]
AD14	VSS
AD15	DDR_CK_N[0]
AD16	DDR_ERR_N
AD17	DDR_ATB0
AD18	DDR_CS_N[2]
AD19	DDR_ODT[1]
AD20	DDR_DQ[14]
AD21	DDR_DQ[8]
AD22	DDR_DQS_P[1]
AD23	DDR_DQ[5]
AD24	DDR_DQS_N[0]
AD25	VSS

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Table 2-38 Pin List Description (AE)

Pin No.	Signal Name
AE1	VSS
AE2	VSS
AE3	DDR_DQ[24]
AE4	DDR_DQS_P[3]
AE5	DDR_DQ[26]
AE6	DDR_DM_DBI_N[2]
AE7	DDR_DQS_P[2]
AE8	VSS
AE9	DDR_DQ[16]
AE10	DDR_ADR[9]
AE11	DDR_ADR[4]
AE12	DDR_CK_N[1]
AE13	VSS
AE14	DDR_PAR
AE15	DDR_CK_P[0]
AE16	VSS
AE17	DDR_WE_N_ADR14
AE18	VSS
AE19	DDR_CAL
AE20	DDR_DM_DBI_N[1]
AE21	VSS
AE22	DDR_DQS_N[1]
AE23	VSS
AE24	DDR_DQS_P[0]
AE25	VSS

2.7. GPIO

2.7.1. Overview

General Purpose Input/Output (GPIO) is a flexible and software-configurable digital signal. The GPIO ports are used to read and write high-level or low-level status information of the pins, and achieve certain functions indicated in the signals.

2.7.2. Feature

The GPIO of JH-7110 has the following features.

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- Support up to 64 GPIOs
- Individually programmable input/output pins, default to output at reset.
- Each GPIO has a dedicated control signal
- Support separate interrupt with a programmable type (level, edge) and polarity
- All pins with MUX with function pins

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2.7.3. GPIO Functions

JH-7110 provides full multiplexing functions to significantly reduce GPIO pins and complexity.

2.7.3.1. Overview

JH-7110 has in total 64 GPIO ports. Each of the ports can be configured as a General Purpose Input and Output (GPIO) port, or multiplexed for a specific signal.

The JH-7110 GPIO ports have the following features.

- Being configurable in software to be input or output
- Setting the value of a digital output
- Reading the value of a digital output
- Generating an interrupt when the input changes value
- Mux as standardized communication protocols signal (I2C, UART, etc.)

2.7.3.2. Function Description

The following table lists the full multiplexing functions of the IO pins.

Important:
JH-7110 GPIO supports full multiplexing. This means that a GPIO pin can be configured to any function listed from Function 1 to Function 2 in the following table.

Important:
Function 0 is the default function of an IO. The columns from Function 1 to Function 2 are just used to categorize example functions, you can configure any of the following function to an IO.

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Table 2-39 GPIO Function Description

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO0	SYS_GPIO0	The test reset input line for JTAG, Negative				
GPIO1	SYS_GPIO1	The test clock input line for JTAG				
GPIO2	SYS_GPIO2	The *Test Data Input (TDI)* line for JTAG certification				
GPIO3	SYS_GPIO3	The *Test Data Output (TDO)* line for JTAG certification				
GPIO4	SYS_GPIO4	The *Test Mode Selection (TMS)* line for JTAG certification				
GPIO5	SYS_GPIO5	The *Transmit Data (TXD)* line of UART				
GPIO6	SYS_GPIO6	The *Receive Data (RXD)* line of UART			DVP_CLK	DVP clock
GPIO7	SYS_GPIO7	GPIO7	LCD_CLK	LCD data output	DVP_VSYNC	DVP vertical synchronization
GPIO8	SYS_GPIO8	GPIO8	LCD_VSYNC	LCD vertical synchronization	DVP_HSYNC	DVP horizontal synchronization
GPIO9	SYS_GPIO9	The test clock input line for JTAG on HIFI4 (Audio DSP)	LCD_HSYNC	LCD horizontal synchronization	DVP_DATA[0]	DVP data lane
GPIO10	SYS_GPIO10	The *Test Data Input (TDI)* line for JTAG on HIFI4 (Audio DSP)	LCD_DE	LCD *Data Enable (DE)* mode	DVP_DATA[1]	DVP data lane
GPIO11	SYS_GPIO11	The *Test Data Output (TDO)* line for JTAG on HIFI4 (Audio DSP)	LCD_-DATAOUT[0]	LCD data output	DVP_DATA[2]	DVP data lane
GPIO12	SYS_GPIO12	The *Test Mode Selection (TMS)* line for JTAG on HIFI4 (Audio DSP)	LCD_-DATAOUT[1]	LCD data output	DVP_DATA[3]	DVP data lane
GPIO13	SYS_GPIO13	The test reset input line for JTAG on HIFI4 (Audio DSP), Negative	LCD_-DATAOUT[2]	LCD data output	DVP_DATA[4]	DVP data lane
GPIO14	SYS_GPIO14	GPIO14	LCD_-DATAOUT[3]	LCD data output	DVP_DATA[5]	DVP data lane
GPIO15	SYS_GPIO15	GPIO15	LCD_-DATAOUT[4]	LCD data output	DVP_DATA[6]	DVP data lane

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Table 2-39 GPIO Function Description (continued)

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO16	SYS_GPIO16	GPIO16	LCD_-DATAOUT[5]	LCD data output	DVP_DATA[7]	DVP data lane
GPIO17	SYS_GPIO17	GPIO17	LCD_-DATAOUT[6]	LCD data output	DVP_DATA[8]	DVP data lane
GPIO18	SYS_GPIO18	The *Transmit Data (TXD)* line of UART	LCD_-DATAOUT[7]	LCD data output	DVP_DATA[9]	DVP data lane
GPIO19	SYS_GPIO19	The *Receive Data (RXD)* line of UART	LCD_-DATAOUT[8]	LCD data output	DVP_DATA[10]	DVP data lane
GPIO20	SYS_GPIO20	GPIO20	LCD_-DATAOUT[9]	LCD data output	DVP_DATA[11]	DVP data lane
GPIO21	SYS_GPIO21	GPIO21	LCD_-DATAOUT[10]	LCD data output	DVP_CLK	DVP clock
GPIO22	SYS_GPIO22	GPIO22	LCD_-DATAOUT[11]	LCD data output	DVP_VSYNC	DVP vertical synchronization
GPIO23	SYS_GPIO23	GPIO23	LCD_-DATAOUT[12]	LCD data output	DVP_HSYNC	DVP horizontal synchronization
GPIO24	SYS_GPIO24	GPIO24	LCD_-DATAOUT[13]	LCD data output	DVP_DATA[0]	DVP data lane
GPIO25	SYS_GPIO25	GPIO25	LCD_-DATAOUT[14]	LCD data output	DVP_DATA[1]	DVP data lane
GPIO26	SYS_GPIO26	GPIO26	LCD_-DATAOUT[15]	LCD data output	DVP_DATA[2]	DVP data lane
GPIO27	SYS_GPIO27	GPIO27	LCD_-DATAOUT[16]	LCD data output	DVP_DATA[3]	DVP data lane
GPIO28	SYS_GPIO28	GPIO28	LCD_-DATAOUT[17]	LCD data output	DVP_DATA[4]	DVP data lane
GPIO29	SYS_GPIO29	GPIO29	LCD_-DATAOUT[18]	LCD data output	DVP_DATA[5]	DVP data lane
GPIO30	SYS_GPIO30	GPIO30	LCD_-DATAOUT[19]	LCD data output	DVP_DATA[6]	DVP data lane

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Table 2-39 GPIO Function Description (continued)

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO31	SYS_GPIO31	GPIO31	LCD_-DATAOUT[20]	LCD data output	DVP_DATA[7]	DVP data lane
GPIO32	SYS_GPIO32	GPIO32	LCD_-DATAOUT[21]	LCD data output	DVP_DATA[8]	DVP data lane
GPIO33	SYS_GPIO33	GPIO33	LCD_-DATAOUT[22]	LCD data output	DVP_DATA[9]	DVP data lane
GPIO34	SYS_GPIO34	GPIO34	LCD_-DATAOUT[23]	LCD data output	DVP_DATA[10]	DVP data lane
GPIO35	SYS_GPIO35	The reset output line of WDT			DVP_DATA[11]	DVP data lane
GPIO36	SYS_GPIO36	The SCL signal trace of I2C	LCD_CLK	LCD data output	DVP_VSYNC	DVP vertical synchronization
GPIO37	SYS_GPIO37	The SDA signal trace of I2C	LCD_VSYNC	LCD vertical synchronization	DVP_HSYNC	DVP horizontal synchronization
GPIO38	SYS_GPIO38	The SCL signal trace of I2C	LCD_HSYNC	LCD horizontal synchronization	DVP_DATA[0]	DVP data lane
GPIO39	SYS_GPIO39	The SDA signal trace of I2C	LCD_DE	LCD *Data Enable (DE)* mode	DVP_DATA[1]	DVP data lane
GPIO40	SYS_GPIO40	The *Receive Data (RXD)* line of UART	LCD_-DATAOUT[0]	LCD data output	DVP_DATA[2]	DVP data lane
GPIO41	SYS_GPIO41	The *Transmit Data (TXD)* line of UART	LCD_-DATAOUT[1]	LCD data output	DVP_DATA[3]	DVP data lane
GPIO42	SYS_GPIO42	The modem control *Request To Send (RTS)* output line of UART, Negative	LCD_-DATAOUT[2]	LCD data output	DVP_DATA[4]	DVP data lane
GPIO43	SYS_GPIO43	The *Clear To Send (CTS)* modem status of UART, Negative	LCD_-DATAOUT[3]	LCD data output	DVP_DATA[5]	DVP data lane
GPIO44	SYS_GPIO44	The *Receive Data (RXD)* line of UART	LCD_-DATAOUT[4]	LCD data output	DVP_DATA[6]	DVP data lane
GPIO45	SYS_GPIO45	The *Transmit Data (TXD)* line of UART	LCD_-DATAOUT[5]	LCD data output	DVP_DATA[7]	DVP data lane
GPIO46	SYS_GPIO46	The modem control *Request To Send (RTS)* output line of UART, Negative	LCD_-DATAOUT[6]	LCD data output	DVP_DATA[8]	DVP data lane

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Table 2-39 GPIO Function Description (continued)

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO47	SYS_GPIO47	The *Clear To Send (CTS)* modem status of UART, Negative	LCD_-DATAOUT[7]	LCD data output	DVP_DATA[9]	DVP data lane
GPIO48	SYS_GPIO48	The chip select line of SPI, Negative	LCD_-DATAOUT[8]	LCD data output	DVP_DATA[10]	DVP data lane
GPIO49	SYS_GPIO49	The series clock line of SPI	LCD_-DATAOUT[9]	LCD data output	DVP_DATA[11]	DVP data lane
GPIO50	SYS_GPIO50	The *Receive Data (RXD)* line of SPI	LCD_-DATAOUT[10]	LCD data output		
GPIO51	SYS_GPIO51	The *Transmit Data (TXD)* line of SPI	LCD_-DATAOUT[11]	LCD data output		
GPIO52	SYS_GPIO52	The chip select line of SPI, Negative	LCD_-DATAOUT[12]	LCD data output		
GPIO53	SYS_GPIO53	The series clock line of SPI	LCD_-DATAOUT[13]	LCD data output		
GPIO54	SYS_GPIO54	The *Receive Data (RXD)* line of SPI	LCD_-DATAOUT[14]	LCD data output		
GPIO55	SYS_GPIO55	The *Transmit Data (TXD)* line of SPI	LCD_-DATAOUT[15]	LCD data output		
GPIO56	SYS_GPIO56	The chip select line of SPI, Negative	LCD_-DATAOUT[16]	LCD data output		
GPIO57	SYS_GPIO57	The series clock line of SPI	LCD_-DATAOUT[17]	LCD data output		
GPIO58	SYS_GPIO58	The *Receive Data (RXD)* line of SPI	LCD_-DATAOUT[18]	LCD data output		
GPIO59	SYS_GPIO59	The *Transmit Data (TXD)* line of SPI	LCD_-DATAOUT[19]	LCD data output		
GPIO60	SYS_GPIO60	The chip select line of SPI, Negative	LCD_-DATAOUT[20]	LCD data output		
GPIO61	SYS_GPIO61	The series clock line of SPI	LCD_-DATAOUT[21]	LCD data output		

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Table 2-39 GPIO Function Description (continued)

IOPAD	Function 0	Function 0 Description	Function 1	Function 1 Description	Function 2	Function 2 Description
GPIO62	SYS_GPIO62	The *Receive Data (RXD)* line of SPI	LCD_-DATAOUT[22]	LCD data output		
GPIO63	SYS_GPIO63	The *Transmit Data (TXD)* line of SPI	LCD_-DATAOUT[23]	LCD data output		

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2.7.3.3. Full Multiplexing

JH-7110 provides full address multiplexing so that SYS_GPIO from SYS_GPIO0 - SYS_GPIO63 in Function 0 can be configured to any of the following signals:

Table 2-40 Full Multiplexing

Signal	Description	Direction	Type	Connect
hifi4_jtag_tck	The TAP clock signal for JTAG on HIFI4	Input	GPIO/Clock	sys_iomux
hifi4_jtag_tdi	The TAP data input signal for JTAG on HIFI4	Input	GPIO	sys_iomux
hifi4_jtag_tdo	The TAP data output signal for JTAG on HIFI4	Output	GPIO	sys_iomux
hifi4_jtag_tms	The TAP mode switch signal for JTAG on HIFI4	Input	GPIO	sys_iomux
hifi4_jtag_trstn	The TAP reset negative signal for JTAG on HIFI4	Input	GPIO	sys_iomux
cdns_qspi_qspi_csn1	The chip select negative signal for QSPI	Output	GPIO	sys_iomux
uart0_rxd	The data receiving signal for UART0	Input	GPIO	sys_iomux
uart0_txd	The data transmission signal for UART0	Output	GPIO	sys_iomux
uart1_cts_n	The *Clear to Send (CTS)* negative signal for UART1	Input	GPIO	sys_iomux
uart1_rts_n	The *Require to Send (RTS)* negative signal for UART1	Output	GPIO	sys_iomux
uart1_rxd	The data receiving signal for UART1	Input	GPIO	sys_iomux
uart1_txd	The data transmission signal for UART1	Output	GPIO	sys_iomux
uart2_cts_n	The *Clear to Send (CTS)* negative signal for UART2	Input	GPIO	sys_iomux
uart2_rts_n	The *Require to Send (RTS)* negative signal for UART2	Output	GPIO	sys_iomux
uart2_rxd	The data transmission signal for UART2	Input	GPIO	sys_iomux
uart2_txd	The data transmission signal for UART2	Output	GPIO	sys_iomux
i2c0_i2c_scl	The clock signal for I2C0	Input/Output	GPIO	sys_iomux
i2c0_i2c_sda	The data transmission signal for I2C0	Input/Output	GPIO	sys_iomux
i2c1_i2c_scl	The clock signal for I2C1	Input/Output	GPIO	sys_iomux
i2c1_i2c_sda	The data transmission signal for I2C1	Input/Output	GPIO	sys_iomux
i2c2_i2c_scl	The clock signal for I2C2	Input/Output	GPIO	sys_iomux
i2c2_i2c_sda	The data transmission signal for I2C2	Input/Output	GPIO	sys_iomux

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Table 2-40 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
tdm_rx	The receiving signal for TDM	Input	GPIO	sys_iomux
tdm_sync	The synchronization signal for TDM	Input/Output	GPIO	sys_iomux
tdm_tx	The transmission signal for TDM	Output	GPIO	sys_iomux
pdm_4mic_dmic0_din	The data input signal for PDM DMIC0	Input	GPIO	sys_iomux
pdm_4mic_dmic1_din	The data input signal for PDM DMIC1	Input	GPIO	sys_iomux
pdm_4mic_dmic_clk	The clock signal for PDM DMIC	Output	GPIO	sys_iomux
uart3_rxd	The data receiving signal for UART3	Input	GPIO	sys_iomux
uart3_txd	The data transmission signal for UART3	Output	GPIO	sys_iomux
uart4_cts_n	The *Clear to Send (CTS)* negative signal for UART4	Input	GPIO	sys_iomux
uart4_rts_n	The *Require to Send (RTS)* negative signal for UART4	Output	GPIO	sys_iomux
uart4_rxd	The data receiving signal for UART3	Input	GPIO	sys_iomux
uart4_txd	The data transmission signal for UART4	Output	GPIO	sys_iomux
uart5_cts_n	The *Clear to Send (CTS)* negative signal for UART5	Input	GPIO	sys_iomux
uart5_rts_n	The *Require to Send (RTS)* negative signal for UART5	Output	GPIO	sys_iomux
uart5_rxd	The data receiving signal for UART5	Input	GPIO	sys_iomux
uart5_txd	The data transmission signal for UART5	Output	GPIO	sys_iomux
i2c3_scl	The clock signal for I2C3	Input/Output	GPIO	sys_iomux
i2c3_sda	The data transmission signal for I2C3	Input/Output	GPIO	sys_iomux
i2c4_scl	The clock signal for I2C4	Input/Output	GPIO	sys_iomux
i2c4_sda	The data transmission signal for I2C4	Input/Output	GPIO	sys_iomux
i2c5_scl	The clock signal for I2C5	Input/Output	GPIO	sys_iomux
i2c5_sda	The data transmission signal for I2C5	Input/Output	GPIO	sys_iomux
i2c6_scl	The clock signal for I2C6	Input/Output	GPIO	sys_iomux
i2c6_sda	The data transmission signal for I2C6	Input/Output	GPIO	sys_iomux

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Table 2-40 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
spi0_ssp_sclk	The clock signal for SPI0	Input/Output	GPIO	sys_iomux
spi0_ssp_csn	The chip select negative signal for SPI0	Input/Output	GPIO	sys_iomux
spi0_ssp_rxd	The data receiving signal for SPI0	Input	GPIO	sys_iomux
spi0_ssp_txd	The data transmission signal for SPI0	Output	GPIO	sys_iomux
spi1_ssp_sclk	The clock signal for SPI1	Input/Output	GPIO	sys_iomux
spi1_ssp_csn	The chip select negative signal for SPI1	Input/Output	GPIO	sys_iomux
spi1_ssp_rxd	The data receiving signal for SPI1	Input	GPIO	sys_iomux
spi1_ssp_txd	The data transmission signal for SPI1	Output	GPIO	sys_iomux
spi2_ssp_sclk	The clock signal for SPI2	Input/Output	GPIO	sys_iomux
spi2_ssp_csn	The chip select negative signal for SPI2	Input/Output	GPIO	sys_iomux
spi2_ssp_rxd	The data receiving signal for SPI2	Input	GPIO	sys_iomux
spi2_ssp_txd	The data transmission signal for SPI2	Output	GPIO	sys_iomux
spi3_ssp_sclk	The clock signal for SPI3	Input/Output	GPIO	sys_iomux
spi3_ssp_csn	The chip select negative signal for SPI3	Input/Output	GPIO	sys_iomux
spi3_ssp_rxd	The data receiving signal for SPI3	Input	GPIO	sys_iomux
spi3_ssp_txd	The data transmission signal for SPI3	Output	GPIO	sys_iomux
spi4_ssp_sclk	The clock signal for SPI4	Input/Output	GPIO	sys_iomux
spi4_ssp_csn	The chip select negative signal for SPI4	Input/Output	GPIO	sys_iomux
spi4_ssp_rxd	The data receiving signal for SPI4	Input	GPIO	sys_iomux
spi4_ssp_txd	The data transmission signal for SPI4	Output	GPIO	sys_iomux
spi5_ssp_sclk	The clock signal for SPI5	Input/Output	GPIO	sys_iomux
spi5_ssp_csn	The chip select negative signal for SPI5	Input/Output	GPIO	sys_iomux
spi5_ssp_rxd	The data receiving signal for SPI5	Input	GPIO	sys_iomux
spi5_ssp_txd	The data transmission signal for SPI5	Output	GPIO	sys_iomux

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Table 2-40 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
spi6_ssp_sclk	The clock signal for SPI6	Input/Output	GPIO	sys_iomux
spi6_ssp_csn	The chip select negative signal for SPI6	Input/Output	GPIO	sys_iomux
spi6_ssp_rxd	The data receiving signal for SPI6	Input	GPIO	sys_iomux
spi6_ssp_txd	The data transmission signal for SPI6	Output	GPIO	sys_iomux
pwm[0]	The PWM 0 signal	Output	GPIO	sys_iomux
pwm[1]	The PWM 1 signal	Output	GPIO	sys_iomux
pwm[2]	The PWM 2 signal	Output	GPIO	sys_iomux
pwm[3]	The PWM 3 signal	Output	GPIO	sys_iomux
pwm[4]	The PWM 4 signal	Output	GPIO	aon_iomux
pwm[5]	The PWM 5 signal	Output	GPIO	aon_iomux
pwm[6]	The PWM 6 signal	Output	GPIO	aon_iomux
pwm[7]	The PWM 7 signal	Output	GPIO	aon_iomux
sys_crg_clk_jtag_tck	The TAP clock signal for JTAG on System CRG clock	Input	GPIO	sys_iomux
clkrst_src_bypass_jtag_trstn	The TAP reset negative signal for JTAG on clock reset source by-pass	Input	GPIO	sys_iomux
jtag_certification_tdi	The TAP data input signal for JTAG on Certification	Input	GPIO	sys_iomux
jtag_certification_tdo	The TAP data output signal for JTAG on Certification	Output	GPIO	sys_iomux
jtag_certification_tms	The TAP mode switch signal for JTAC on Certification	Input	GPIO	sys_iomux
sdio0_back_end_power	The back end power signal for SDIO0	Output	GPIO	sys_iomux
sdio0_card_int_n	The card initialization negative signal for SDIO0	Input	GPIO	sys_iomux
sdio0_card_power_en	The card power supply signal for SDIO0	Output	GPIO	sys_iomux
sdio0_card_write_prt	The card data write signal for SDIO0	Input	GPIO	sys_iomux
sdio0_card_rst_n	The card reset negative signal for SDIO0	Output	GPIO	sys_iomux
sdio0_ccmd_od_pullup_en_n	The pullup enable signal for SDIO0	Output	GPIO	sys_iomux
sdio0_card_detect_n	The card detect negative signal for SDIO0	Input	GPIO	sys_iomux

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Table 2-40 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
sdio1_back_end_power	The back end power signal for SDIO1	Output	GPIO	sys_iomux
sdio1_card_int_n	The card initialization negative signal for SDIO1	Input	GPIO	sys_iomux
sdio1_card_power_en	The card power supply signal for SDIO1	Output	GPIO	sys_iomux
sdio1_card_write_prt	The card data write signal for SDIO1	Input	GPIO	sys_iomux
sdio1_clk	The clock signal for SDIO1	Output	GPIO	sys_iomux
sdio1_ccmd	The Command signal of SDIO1	Input/Output	GPIO	sys_iomux
sdio1_cdata[0]	The Data 0 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[1]	The Data 1 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[2]	The Data 2 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[3]	The Data 3 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[4]	The Data 4 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[5]	The Data 5 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[6]	The Data 6 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_cdata[7]	The Data 7 signal of SDIO0	Input/Output	GPIO	sys_iomux
sdio1_card_rst_n	The card reset signal of SDIO1	Output	GPIO	sys_iomux
sdio1_ccmd_od_pullup_en_n	The pullup enable signal for SDIO1	Output	GPIO	sys_iomux
sdio1_data_strobe	The data strobe signal for SDIO1	Input	GPIO	sys_iomux
sdio1_card_detect_n	The card detect signal for SDIO1	Input	GPIO	sys_iomux
sys_crg_ext_mclk	The external main clock signal for System CRG.	Input	GPIO	sys_iomux
sys_crg_mclk_out	The main clock output signal for System CRG.	Output	GPIO	sys_iomux
sys_crg_clk_gmac_phy	The GMAC PHY signal for System CRG.	Output	GPIO	sys_iomux
sys_crg_i2stx_bclk_mst	The bit clock master signal for I2S Transmission	Output	GPIO	sys_iomux
sys_crg_i2stx_lrck_mst	The left-right clock (frame clock) master signal for I2S Transmission	Output	GPIO	sys_iomux
sys_crg_i2srx_bclk_mst	The bit clock master signal for I2S Receiving	Output	GPIO	sys_iomux

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Table 2-40 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
sys_crg_i2srx_lrck_mst	The left-right clock (frame clock) master signal for I2S Receiving	Output	GPIO	sys_iomux
sys_crg_i2stx_bclk_slv	The bit clock slave signal for I2S Transmission	Input	GPIO	sys_iomux
sys_crg_i2stx_lrck_slv	The left-right clock (frame clock) slave signal for I2S Transmission	Input	GPIO	sys_iomux
sys_crg_i2srx_bclk_slv	The bit clock slave signal for I2S Receiving	Input	GPIO	sys_iomux
sys_crg_i2srx_lrck_slv	The left-right clock (frame clock) slave signal for I2S Receiving	Input	GPIO	sys_iomux
sys_crg_tdm_clk_slv	The TDM slave clock signal for System CRG	Input	GPIO	sys_iomux
sys_crg_tdm_clk_mst	The TDM master clock signal for System CRG	Output	GPIO	sys_iomux
aon_crg_clk_32k_out	The clock 32K output signal for AON CRG	Output	GPIO	aon_iomux
i2stx_4ch_sdo0	The Sound Output 0 for I2S	Output	GPIO	sys_iomux
i2stx_4ch_sdo1	The Sound Output 1 for I2S	Output	GPIO	sys_iomux
i2stx_4ch_sdo2	The Sound Output 2 for I2S	Output	GPIO	sys_iomux
i2stx_4ch_sdo3	The Sound Output 3 for I2S	Output	GPIO	sys_iomux
audio_i2srx_ext_sdin0	The Sound Input 0 for I2S	Input	GPIO	sys_iomux
audio_i2srx_ext_sdin1	The Sound Input 1 for I2S	Input	GPIO	sys_iomux
audio_i2srx_ext_sdin2	The Sound Input 2 for I2S	Input	GPIO	sys_iomux
sys_crg_clk_gclk0	The Global Clock 0 signal for System CRG	Output	GPIO	aon_iomux
sys_crg_clk_gclk1	The Global Clock 1 signal for System CRG	Output	GPIO	aon_iomux
sys_crg_clk_gclk2	The Global Clock 2 signal for System CRG	Output	GPIO	aon_iomux
spdif_spdifi	The input signal for SPDIF	Input	GPIO	sys_iomux
spdif_spdifo	The output signal for SPDIF	Output	GPIO	sys_iomux
vout_hdmi_tx_cec_sda	The serial data CEC signal for HDMI Transmission	Input/Output	GPIO	sys_iomux
vout_hdmi_tx_ddc_scl	The serial clock DDC signal for HDMI Transmission	Input/Output	GPIO	sys_iomux
vout_hdmi_tx_ddc_sda	The serial data DDC signal for HDMI Transmission	Input/Output	GPIO	sys_iomux
vout_hdmi_tx_hdmitx_hpd	The *Hot Plug Detect (HPD)* signal for HDMI Transmission	Input	GPIO	sys_iomux

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Table 2-40 Full Multiplexing (continued)

Signal	Description	Direction	Type	Connect
usb_drive_vbus_io	The VBUS (power supply + cable) input/output signal for USB	Output	GPIO	sys_iomux
usb_overcurrent_n_io	The over-current input/output signal for USB	Input	GPIO	sys_iomux
u7mc_sft7110_tref	The Timer Reference signal for U74 MC	Output	GPIO	sys_iomux
u7mc_sft7110_tdata[0]	The Timer Data 0 signal for U74 MC	Output	GPIO	sys_iomux
u7mc_sft7110_tdata[1]	The Timer Data 1 signal for U74 MC	Output	GPIO	sys_iomux
u7mc_sft7110_tdata[2]	The Timer Data 2 signal for U74 MC	Output	GPIO	sys_iomux
u7mc_sft7110_tdata[3]	The Timer Data 3 signal for U74 MC	Output	GPIO	sys_iomux
WAVE511_i_uart_rxsin	The UART receiving input signal for WAVE511	Input	GPIO	sys_iomux
WAVE511_o_uart_txsout	The UART transmission input signal for WAVE511	Output	GPIO	sys_iomux
GPIO_wakeup[3]	The GPIO Wakeup 3 signal	Input	GPIO	aon_iomux
GPIO_wakeup[2]	The GPIO Wakeup 2 signal	Input	GPIO	aon_iomux
GPIO_wakeup[1]	The GPIO Wakeup 1 signal	Input	GPIO	aon_iomux
GPIO_wakeup[0]	The GPIO Wakeup 0 signal	Input	GPIO	aon_iomux
can_ctrl0_can_txd	The data transmission signal for CAN Controller 0	Output	GPIO	sys_iomux
can_ctrl0_can_rxd	The data receiving signal for CAN Controller 0	Input	GPIO	sys_iomux
can_ctrl1_can_stby	The standby signal for CAN Controller 1	Output	GPIO	sys_iomux
can_ctrl1_can_txd	The data transmission signal for CAN Controller 1	Output	GPIO	sys_iomux
can_ctrl1_can_rxd	The data receiving signal for CAN Controller 1	Input	GPIO	sys_iomux
can_ctrl1_can_stby	The standby signal for CAN Controller 1	Output	GPIO	sys_iomux
can_ctrl0_tst_sample_point	The test sample point for CAN Controller 0	Output	GPIO	sys_iomux
can_ctrl0_tst_next_bit	The test next point for CAN Controller 0	Output	GPIO	sys_iomux
can_ctrl1_tst_sample_point	The test sample point for CAN Controller 1	Output	GPIO	sys_iomux
can_ctrl1_tst_next_bit	The test next point for CAN Controller 1	Output	GPIO	sys_iomux
dskit_wdt_rstout	The reset output signal for WDT	Output	GPIO	sys_iomux

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2.7.4. GPIO Output Signals

The StarFive JH-7110 Datasheet has listed the fundamental GPIO multiplexing descriptions, besides this, the following tables list the complete GPIO output signals and the configuration instructions.

Note:
To set the GPIO input and output signals, see instructions in the Software SDK Developer Guide for GPIO for more information.

Table 2-41 GPIO OEN List for SYS_IOMUX

Index	Output	OEN	Description
0	1'd0	1'd0	Use the index value to set the register as low level output.
1	1'd1	1'd1	Use the index value to set the register as high level output.
2	U0_WAVE511_UART_TXSOUT	u0_dom_vout_top_u0_hdmi_tx_pin_cec_sda_oen	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
3	U0_CAN_CTRL_STBY	u0_dom_vout_top_u0_hdmi_tx_pin_ddc_scl_oen	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
4	U0_CAN_CTRL_TST_NEXT_BIT	u0_dom_vout_top_u0_hdmi_tx_pin_ddc_sda_oen	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
5	u0_can_ctrl_tst_sample_point	u0_i2c_ic_clk_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
6	u0_can_ctrl_txd	u0_i2c_ic_data_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
7	u0_cdn_usb_drive_vbus_io	u0_hifi4_JTDOEn	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
8	u0_cdns_qspi_csn1	u0_jtag_certification_tdo_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
9	u0_cdns_spdif_spdifo	u0_pwm_8ch_ptc_oe_n[0]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
10	u0_dom_vout_top_u0_-hdmi_tx_pin_cec_sda_out	u0_pwm_8ch_ptc_oe_-n[1]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
11	u0_dom_vout_top_u0_-hdmi_tx_pin_ddc_scl_out	u0_pwm_8ch_ptc_oe_-n[2]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
12	u0_dom_vout_top_u0_-hdmi_tx_pin_ddc_sda_-out	u0_pwm_8ch_ptc_oe_-n[3]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
13	u0_dskit_wdt_WDOGRES	u0_ssp_spi_nSSPCTLOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
14	u0_i2c_ic_clk_out_a	u0_ssp_spi_nSSPOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
15	u0_i2c_ic_data_out_a	u0_tdm16slot_nPCM_-SYNCOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
16	u0_sdio_back_end_power	u0_tdm16slot_nPCM_TX-DOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
17	u0_sdio_card_power_en	u1_i2c_ic_clk_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
18	u0_sdio_ccmd_od_-pullup_en_n	u1_i2c_ic_data_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
19	u0_sdio_rst_n	u1_sdio_ccmd_out_en	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
20	u0_uart_sout	u1_sdio_cdata_out_en[0]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
21	u0_hifi4_JTDO	u1_sdio_cdata_out_en[1]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
22	u0_jtag_certification_tdo	u1_sdio_cdata_out_en[2]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
23	u0_pdm_4mic_dmic_mclk	u1_sdio_cdata_out_en[3]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
24	u0_pwm_8ch_ptc_p-wm[0]	u1_sdio_cdata_out_en[4]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
25	u0_pwm_8ch_ptc_p-wm[1]	u1_sdio_cdata_out_en[5]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
26	u0_pwm_8ch_ptc_p-wm[2]	u1_sdio_cdata_out_en[6]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
27	u0_pwm_8ch_ptc_p-wm[3]	u1_sdio_cdata_out_en[7]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
28	u0_pwmdac_pwmdac_-left_output	u1_ssp_spi_nSSPCTLOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
29	u0_pwmdac_pwmdac_-right_output	u1_ssp_spi_nSSPOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
30	u0_ssp_spi_SSPCLKOUT	u2_i2c_ic_clk_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
31	u0_ssp_spi_SSPFSSOUT	u2_i2c_ic_data_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
32	u0_ssp_spi_SSPTXD	u2_ssp_spi_nSSPCTLOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
33	u0_sys_crg_clk_gmac_phy	u2_ssp_spi_nSSPOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
34	u0_sys_crg_i2srx_bclk_mst	u3_i2c_ic_clk_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
35	u0_sys_crg_i2srx_lrck_mst	u3_i2c_ic_data_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
36	u0_sys_crg_i2stx_bclk_mst	u3_ssp_spi_nSSPCTLOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
37	u0_sys_crg_i2stx_lrck_mst	u3_ssp_spi_nSSPOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
38	u0_sys_crg_mclk_out	u4_i2c_ic_clk_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
39	u0_sys_crg_tdm_clk_mst	u4_i2c_ic_data_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
40	u0_tdm16slot_PCM_SYNCOUT	u4_ssp_spi_nSSPCTLOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
41	u0_tdm16slot_PCM_TXD	u4_ssp_spi_nSSPOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
42	u0_u7mc_sft7110_trace_com_pib_tdata[0]	u5_i2c_ic_clk_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
43	u0_u7mc_sft7110_trace_com_pib_tdata[1]	u5_i2c_ic_data_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
44	u0_u7mc_sft7110_trace_com_pib_tdata[2]	u5_ssp_spi_nSSPCTLOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
45	u0_u7mc_sft7110_trace_com_pib_tdata[3]	u5_ssp_spi_nSSPOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
46	u0_u7mc_sft7110_trace_-com_pib_tref	u6_i2c_ic_clk_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
47	u1_can_ctrl_stby	u6_i2c_ic_data_oe	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
48	u1_can_ctrl_tst_next_bit	u6_ssp_spi_nSSPCTLOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
49	u1_can_ctrl_tst_sample_-point	u6_ssp_spi_nSSPOE	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
50	u1_can_ctrl_txd		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
51	u1_i2c_ic_clk_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
52	u1_i2c_ic_data_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
53	u1_sdio_back_end_power		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
54	u1_sdio_card_power_en		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
55	u1_sdio_cclk_out		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
56	u1_sdio_ccmd_od_-pullup_en_n		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
57	u1_sdio_ccmd_out		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
58	u1_sdio_cdata_out[0]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
59	u1_sdio_cdata_out[1]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
60	u1_sdio_cdata_out[2]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
61	u1_sdio_cdata_out[3]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
62	u1_sdio_cdata_out[4]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
63	u1_sdio_cdata_out[5]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
64	u1_sdio_cdata_out[6]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
65	u1_sdio_cdata_out[7]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
66	u1_sdio_rst_n		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
67	u1_uart_rts_n		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
68	u1_uart_sout		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
69	u1_i2stx_4ch_sdo0		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
70	u1_i2stx_4ch_sdo1		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
71	u1_i2stx_4ch_sdo2		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
72	u1_i2stx_4ch_sdo3		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
73	u1_ssp_spi_SSPCLKOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
74	u1_ssp_spi_SSPFSSOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
75	u1_ssp_spi_SSPTXD		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
76	u2_i2c_ic_clk_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
77	u2_i2c_ic_data_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
78	u2_uart_rts_n		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
79	u2_uart_sout		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
80	u2_ssp_spi_SSPCLKOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
81	u2_ssp_spi_SSPFSSOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
82	u2_ssp_spi_SSPTXD		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
83	u3_i2c_ic_clk_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
84	u3_i2c_ic_data_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
85	u3_uart_sout		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
86	u3_ssp_spi_SSPCLKOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
87	u3_ssp_spi_SSPFSSOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
88	u3_ssp_spi_SSPTXD		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
89	u4_i2c_ic_clk_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
90	u4_i2c_ic_data_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
91	u4_uart_rts_n		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
92	u4_uart_sout		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
93	u4_ssp_spi_SSPCLKOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
94	u4_ssp_spi_SSPFSSOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
95	u4_ssp_spi_SSPTXD		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
96	u5_i2c_ic_clk_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
97	u5_i2c_ic_data_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
98	u5_uart_rts_n		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
99	u5_uart_sout		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
100	u5_ssp_spi_SSPCLKOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
101	u5_ssp_spi_SSPFSSOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
102	u5_ssp_spi_SSPTXD		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
103	u6_i2c_ic_clk_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
104	u6_i2c_ic_data_out_a		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
105	u6_ssp_spi_SSPCLKOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-41 GPIO OEN List for SYS_IOMUX (continued)

Index	Output	OEN	Description
106	u6_ssp_spi_SSPFSSOUT		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
107	u6_ssp_spi_SSPTXD		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

Table 2-42 GPIO OEN List for AON_IOMUX

Index	Output	OEN	Description
0	1'd0	1'd0	Use the index value to set the register as low level output.
1	1'd1	1'd1	Use the index value to set the register as high level output.
2	u0_aon_crg_clk_32k_out	u0_pwm_8ch_ptc_oe_n[4]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
3	u0_pwm_8ch_ptc_pwm[4]	u0_pwm_8ch_ptc_oe_n[5]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
4	u0_pwm_8ch_ptc_pwm[5]	u0_pwm_8ch_ptc_oe_n[6]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
5	u0_pwm_8ch_ptc_pwm[6]	u0_pwm_8ch_ptc_oe_n[7]	Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
6	u0_pwm_8ch_ptc_pwm[7]		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
7	u0_sys_crg_clk_gclk0		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.
8	u0_sys_crg_clk_gclk1		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

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Table 2-42 GPIO OEN List for AON_IOMUX (continued)

Index	Output	OEN	Description
9	u0_sys_crg_clk_gclk2		Use the index value to set the register as an input or an output signal. See Configuring for General Purpose *(on page 120)* for more instructions.

Note:
The index value column lists the enumeration values in GPIO settings, you can use it to set the GPIO registers. For example, to configure the signal ″u6_ssp_spi_SSPTXD″, write "107" in the corresponding register.

2.7.5. GPIO Input Signals

The StarFive JH-7110 Datasheet has listed the fundamental GPIO multiplexing descriptions, besides this, the following table lists the complete GPIO input signals and the configuration instructions.

Note:
To set the GPIO input and output signals, see instructions in the Software SDK Developer Guide for GPIO for more information.

Signal	Direction	Type	Connect	Description
HIFI4_JTAG_TCK	Input	GPIO/clock	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
HIFI4_JTAG_TCK_TDI	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
HIFI4_JTAG_TMS	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
HIFI4_JTAG_TRSTN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_UART_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.

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Signal	Direction	Type	Connect	Description
U1_UART_CTS_N	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_UART_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U2_UART_CTS_N	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U2_UART_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
TDM_RX	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
DMIC0_DIN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
DMIC1_DIN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U3_UART_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U4_UART_CTS_N	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since

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Signal	Direction	Type	Connect	Description
				they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U4_UART_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U5_UART_CTS_N	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U5_UART_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_SSP_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_SSP_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U2_SSP_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U3_SSP_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U4_SSP_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for

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Signal	Direction	Type	Connect	Description
				General Purpose *(on page 120)* for more instructions.
U5_SSP_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U6_SSP_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SYS_CLK_JTAG	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
JTAG_TRSTN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
JTAG_CERTIFICATION_TDI	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
JTAG_CERTIFICATION_TMS	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_SDIO_CARD_INIT_N	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_SDIO_CARD_WRITE_PRT	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.

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Signal	Direction	Type	Connect	Description
U0_SDIO_CARD_DETECT_N	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_SDIO_CARD_INIT_N	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_SDIO_CARD_WRITE_PRT	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_SDIO_DATA_STROBE	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_SDIO_CARD_DETECT_N	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SYS_EXT_MCLK	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SYS_I2STX_BCLK_SLV	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SYS_I2STX_LRCK_SLV	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SYS_I2SRX_BCLK_SLV	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since

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Signal	Direction	Type	Connect	Description
				they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SYS_I2SRX_LRCK_SLV	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SYS_TDM_CLK_SLV	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
AUDIO_I2SRX_EXT_SDIN0	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
AUDIO_I2SRX_EXT_SDIN1	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
AUDIO_I2SRX_EXT_SDIN2	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SPDIF_SPDIFI	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
VOUT_HDMI_TX_HPD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
USB_OVERCURRENT_N_IO	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for

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Signal	Direction	Type	Connect	Description
				General Purpose *(on page 120)* for more instructions.
WAVE511_UART_RXSIN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_CAN_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_CAN_RXD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_I2C_SCL	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_I2C_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_I2C_SCL	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_I2C_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U2_I2C_SCL	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.

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Signal	Direction	Type	Connect	Description
U2_I2C_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
TDM_SYNC	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U3_I2C_SCL	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U3_I2C_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U4_I2C_SCL	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U4_I2C_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U5_I2C_SCL	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U5_I2C_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U6_I2C_SCL	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since

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Signal	Direction	Type	Connect	Description
				they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U6_I2C_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_SPI_SCLK	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U0_SPI_CSN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_SPI_SCLK	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U1_SPI_CSN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U2_SPI_SCLK	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U2_SPI_CSN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U3_SPI_SCLK	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for

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Signal	Direction	Type	Connect	Description
				General Purpose *(on page 120)* for more instructions.
U3_SPI_CSN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U4_SPI_SCLK	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U4_SPI_CSN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U5_SPI_SCLK	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U5_SPI_CSN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U6_SPI_SCLK	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
U6_SPI_CSN	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SDIO_CCMD	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.

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Signal	Direction	Type	Connect	Description
SDIO_CDATA[0]	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SDIO_CDATA[1]	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SDIO_CDATA[2]	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SDIO_CDATA[3]	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SDIO_CDATA[4]	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SDIO_CDATA[5]	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SDIO_CDATA[6]	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
SDIO_CDATA[7]	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
VOUT_HDMI_TX _CEC_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since

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Signal	Direction	Type	Connect	Description
				they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
VOUT_HDMI_TX _DDC_SCL	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
VOUT_HDMI_TX _DDC_SDA	Input	GPIO	SYS IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
GPIO_Wakeup[3]	Input	GPIO	AON IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
GPIO_Wakeup[2]	Input	GPIO	AON IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
GPIO_Wakeup[1]	Input	GPIO	AON IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.
GPIO_Wakeup[0]	Input	GPIO	AON IOMUX	Different from the output signals, the input signals does not have a corresponding index value since they are always configurable. See Configuring for General Purpose *(on page 120)* for more instructions.

2.7.6. GPIO Programming Reference

JH-7110 has in total 64 GPIO ports. Each of the ports can be configured as a General Purpose Input and Output (GPIO) port, or multiplexed for a specific signal.

JH7110 has separate input and output signals, for some GPIO pins, users can set them as input and output at the same time, while for the others, they can't, see the following 2 topics for more details.

- GPIO Output Signals *(on page 97)*
- GPIO Input Signals *(on page 107)*

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2.7.6.1. GPIO Functions

The GPIO ports of JH-7110 has the following functions.

- Being configurable in software to be input or output
- Setting the value of a digital output
- Reading the value of a digital output
- Generating an interrupt when the input changes value
- Mux as standardized communication protocols signal (I2C, UART, etc.)

2.7.6.2. GPIO Registers

2.7.6.2.1. SYS IOMUX CFG

See SYS IOMUX CFG *(on page 320)* for a complete list of all the relevant registers and their respective descriptions.

SYS IOMUX CFG is used to configure the GPIO ports, the register map is shown as follows.

```
typedef struct
{
    __IO uint32_t doen[16];
    __IO uint32_t dout[16];
    __IO uint32_t sig_in[23];
    __IO uint32_t en;
    __IO uint32_t is[2];
    __IO uint32_t ic[2];
    __IO uint32_t ibe[2];
    __IO uint32_t iev[2];
    __IO uint32_t ie[2];
    __I  uint32_t ris[2];
    __I  uint32_t mis[2];
    __I  uint32_t din[2];
} sys_gpio_regs_t;
```

2.7.6.2.2. AON IOMUX CFG

See AON IOMUX CFG *(on page 468)* for a complete list of all the relevant registers and their respective descriptions.

AON IOMUX CFG is used to configure the RGPIO ports, the register map is shown as follows.

```
typedef struct
{
    __IO uint32_t doen;
    __IO uint32_t dout;
    __IO uint32_t sig_in;
    __IO uint32_t en;
    __IO uint32_t is;
    __IO uint32_t ic;
    __IO uint32_t ibe;
    __IO uint32_t iev;
    __IO uint32_t ie;
    __I  uint32_t ris;
    __I  uint32_t mis;
    __I  uint32_t din;
} sys_rgpio_regs_t;
```

2.7.6.3. Programming Examples

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2.7.6.3.1. Configuring for General Purpose

Basically you can configure a GPIO port either for input or for output, the topic provides examples on the configuration.

Configuring for Output

The following code block provides an example of configuring GPIO11 as an output port.

```
port = 11;
n = port >> 2;
shift = ((port & 0x3) << 3);
//direction = output
modl(regs->doen+n, GPIO_DOEN_MASK<<shift, 0<<shift);
//pull up
modl(regs->dout+n, GPIO_DOUT_MASK<<shift, 1<<shift);
//pull down
modl(regs->dout+n, GPIO_DOUT_MASK<<shift, 0<<shift);
```

Configuring for Input

The following code block provides an example of configuring GPIO12 as an input port.

```
port = 12;
n = port >> 2;
shift = ((port & 0x3) << 3);
// direction = input
modl(regs->doen+n, GPIO_DOEN_MASK<<shift, 1<<shift);

// connect 3.3V to pull up, or GND to pull down.

value = (regs->din[port>>5] >> (port & 0x1F)) & 0x1;
```

2.7.6.3.2. Configuring for Special Purpose

Basic Rules

Besides the general input or output functions, you can also use StarFive's pin multiplexing (PINMUX) technologies to configure a GPIO port for special signaling.

There are 3 types of signals: GPO, GPI and GPEN. Different function may require different types of signals.

The basic rules are shown as follow:

Table 2-44 Basic PINMUX Rules

Function	GPO Signal	GPI Signal	GPEN Signal
Unidirectional input	None	Required	May require
Unidirectional output	Required	None	May require
Bidirectional input/output	Required	Required	Required

The following list provides more explanation of the signals.

- GPO Signal - The GPO signal is required for the output function.
- GPI Signal - The GPI signal is required for the input function.
- GPEN - The GPEN signal is the output enabling signal.

To complete the PINMUX, you need to configure signal index in the register. For more information on the signal index, see Signal Index Table *(on page 126)*.

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It's worth noting that not all functions have dedicated GPEN signals. For the input function without a GPEN signal, the index value should be fixed to 1. For the output function without a GPEN signal, the index value should be fixed to 0. In the following programming example, the index of the GPEN signal is denoted as OEN.

If GPO signal is required, regs->dout should be configured.

```
gpo; //GPO signal index
n = port >> 2;
shift = (port & 0x3) << 3;
modl(regs->dout+n, GPIO_DOUT_MASK<<shift, gpo<<shift);
```

If GPEN signal is required, regs->doen should be configured.

```
oen; //GPEN signal index
n = port >> 2;
shift = ((port & 0x3) << 3);
modl(regs->doen+n, GPIO_DOEN_MASK<<shift, oen<<shift);
```

If GPI signal is required, regs->sig_in should be configured.

```
gpi; //GPI signal index
n = gpi >> 2;
shift = ((gpi & 0x3) << 3);
modl(regs->sig_in+n, GPIO_SIG_IN_MASK<<shift, (port+2)<<shift);
```

Configuring a GPIO as UART Signal

The following code block provides an example of configuring GPIO11 as UART0 RX.

```
GPI signal: GPI_SYS_IOMUX_U0_DW_UART_SIN (index 14)
GPO signal: none
GPEN signal: none

port = 11;
gpi = 14; //GPI signal index
oen = 1; //no GPEN signal, but it's an input function, fixed to 1

n = gpi >> 2;
shift = ((gpi & 0x3) << 3);
modl(regs->sig_in+n, GPIO_SIG_IN_MASK<<shift, (port+2)<<shift);

n = port >> 2;
shift = ((port & 0x3) << 3);
modl(regs->doen+n, GPIO_DOEN_MASK<<shift, oen<<shift);
```

Configuring a GPIO as SDIO Signal

The following code block provides an example of configuring GPIO12 as SDIO1 DATA0.

```
GPI signal: GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_0 (index 45)
GPO signal: GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_0 (index 58)
GPEN signal: GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_0 (index 20)

port = 12;
gpi = 45; //GPI signal index
gpo = 58; //GPO signal index
oen = 20; //GPEN signal index

n = gpi >> 2;
shift = (gpi & 3) << 3;
modl(regs->sig_in+n, GPIO_SIG_IN_MASK<<shift, (gpio+2)<<shift);

n = port >> 2;
shift = (port & 0x3) << 3;
modl(regs->dout+n, GPIO_DOUT_MASK<<shift, gpo<<shift);
modl(regs->doen+n, GPIO_DOEN_MASK<<shift, oen<<shift);
```

2.7.6.3.3. GPIO Interrupts

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JH-7110 supports the following 5 interrupt trigger modes.

- High trigger
- Low trigger
- Positive edge trigger
- Negative edge trigger
- Both edge trigger

Follow the steps below to configure GPIO interrupts.

1. Configure the **is/ibe/iev** register according to the following table.
2. Clean the **irq** status by writing **ic** register.
3. Write **ie** register to enable the interrupt.

Table 2-45 GPIO Interrupts

Trigger Mode	reg->is	reg->ibe	reg->iev
high trigger	0	0/1	0
low trigger	0	0/1	1
positive edge trigger	1	0	1
negative edge trigger	1	0	0
both edge trigger	1	1	0/1

The following code block provides an example of configuring the positive edge trigger.

```
port = 11;
is = 1; ibe = 0; iev = 1; //positive edge trigger
n = port>>5,
bit = port & 0x1f;
modl(regs->is+n, BIT(bit), is<<bit);
modl(regs->ibe+n, BIT(bit), ibe<<bit);
modl(regs->iev+n, BIT(bit), iev<<bit);
modl(regs->ic+n, BIT(bit), 0);
modl(regs->ic+n, BIT(bit), BIT(bit));
modl(regs->ie+n, BIT(bit), BIT(bit));
```

2.7.6.4. Reference Header

The following code block shows the headers that can be referenced in GPIO configuration.

```
//GPO SYS_IOMUX
#define GPO_SYS_IOMUX_U0_WAVE511_O_UART_TXSOUT 2
#define GPO_SYS_IOMUX_U0_CAN_CTRL_STBY 3
#define GPO_SYS_IOMUX_U0_CAN_CTRL_TST_NEXT_BIT 4
#define GPO_SYS_IOMUX_U0_CAN_CTRL_TST_SAMPLE_POINT 5
#define GPO_SYS_IOMUX_U0_CAN_CTRL_TXD 6
#define GPO_SYS_IOMUX_U0_CDN_USB_DRIVE_VBUS_IO 7
#define GPO_SYS_IOMUX_U0_CDNS_QSPI_CSN1 8
#define GPO_SYS_IOMUX_U0_CDNS_SPDIF_SPDIFO 9
#define GPO_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_CEC_SDA_OUT 10
#define GPO_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SCL_OUT 11
#define GPO_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SDA_OUT 12
#define GPO_SYS_IOMUX_U0_DSKIT_WDT_WDOGRES 13
#define GPO_SYS_IOMUX_U0_DW_I2C_IC_CLK_OUT_A 14
#define GPO_SYS_IOMUX_U0_DW_I2C_IC_DATA_OUT_A 15
#define GPO_SYS_IOMUX_U0_DW_SDIO_BACK_END_POWER 16
#define GPO_SYS_IOMUX_U0_DW_SDIO_CARD_POWER_EN 17
#define GPO_SYS_IOMUX_U0_DW_SDIO_CCMD_OD_PULLUP_EN_N 18
#define GPO_SYS_IOMUX_U0_DW_SDIO_RST_N 19
#define GPO_SYS_IOMUX_U0_DW_UART_SOUT 20
```


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```
#define GPO_SYS_IOMUX_U0_HIFI4_JTDO 21
#define GPO_SYS_IOMUX_U0_JTAG_CERTIFICATION_TDO 22
#define GPO_SYS_IOMUX_U0_PDM_4MIC_DMIC_MCLK 23
#define GPO_SYS_IOMUX_U0_PWM_8CH_PTC_PWM_0 24
#define GPO_SYS_IOMUX_U0_PWM_8CH_PTC_PWM_1 25
#define GPO_SYS_IOMUX_U0_PWM_8CH_PTC_PWM_2 26
#define GPO_SYS_IOMUX_U0_PWM_8CH_PTC_PWM_3 27
#define GPO_SYS_IOMUX_U0_PWMDAC_PWMDAC_LEFT_OUTPUT 28
#define GPO_SYS_IOMUX_U0_PWMDAC_PWMDAC_RIGHT_OUTPUT 29
#define GPO_SYS_IOMUX_U0_SSP_SPI_SSPCLKOUT 30
#define GPO_SYS_IOMUX_U0_SSP_SPI_SSPFSSOUT 31
#define GPO_SYS_IOMUX_U0_SSP_SPI_SSPTXD 32
#define GPO_SYS_IOMUX_U0_SYS_CRG_CLK_GMAC_PHY 33
#define GPO_SYS_IOMUX_U0_SYS_CRG_I2SRX_BCLK_MST 34
#define GPO_SYS_IOMUX_U0_SYS_CRG_I2SRX_LRCK_MST 35
#define GPO_SYS_IOMUX_U0_SYS_CRG_I2STX_BCLK_MST 36
#define GPO_SYS_IOMUX_U0_SYS_CRG_I2STX_LRCK_MST 37
#define GPO_SYS_IOMUX_U0_SYS_CRG_MCLK_OUT 38
#define GPO_SYS_IOMUX_U0_SYS_CRG_TDM_CLK_MST 39
#define GPO_SYS_IOMUX_U0_TDM16SLOT_PCM_SYNCOUT 40
#define GPO_SYS_IOMUX_U0_TDM16SLOT_PCM_TXD 41
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TDATA_0 42
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TDATA_1 43
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TDATA_2 44
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TDATA_3 45
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TREF 46
#define GPO_SYS_IOMUX_U1_CAN_CTRL_STBY 47
#define GPO_SYS_IOMUX_U1_CAN_CTRL_TST_NEXT_BIT 48
#define GPO_SYS_IOMUX_U1_CAN_CTRL_TST_SAMPLE_POINT 49
#define GPO_SYS_IOMUX_U1_CAN_CTRL_TXD 50
#define GPO_SYS_IOMUX_U1_DW_I2C_IC_CLK_OUT_A 51
#define GPO_SYS_IOMUX_U1_DW_I2C_IC_DATA_OUT_A 52
#define GPO_SYS_IOMUX_U1_DW_SDIO_BACK_END_POWER 53
#define GPO_SYS_IOMUX_U1_DW_SDIO_CARD_POWER_EN 54
#define GPO_SYS_IOMUX_U1_DW_SDIO_CCLK_OUT 55
#define GPO_SYS_IOMUX_U1_DW_SDIO_CCMD_OD_PULLUP_EN_N 56
#define GPO_SYS_IOMUX_U1_DW_SDIO_CCMD_OUT 57
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_0 58
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_1 59
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_2 60
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_3 61
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_4 62
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_5 63
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_6 64
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_7 65
#define GPO_SYS_IOMUX_U1_DW_SDIO_RST_N 66
#define GPO_SYS_IOMUX_U1_DW_UART_RTS_N 67
#define GPO_SYS_IOMUX_U1_DW_UART_SOUT 68
#define GPO_SYS_IOMUX_U1_I2STX_4CH_SDO0 69
#define GPO_SYS_IOMUX_U1_I2STX_4CH_SDO1 70
#define GPO_SYS_IOMUX_U1_I2STX_4CH_SDO2 71
#define GPO_SYS_IOMUX_U1_I2STX_4CH_SDO3 72
#define GPO_SYS_IOMUX_U1_SSP_SPI_SSPCLKOUT 73
#define GPO_SYS_IOMUX_U1_SSP_SPI_SSPFSSOUT 74
#define GPO_SYS_IOMUX_U1_SSP_SPI_SSPTXD 75
#define GPO_SYS_IOMUX_U2_DW_I2C_IC_CLK_OUT_A 76
#define GPO_SYS_IOMUX_U2_DW_I2C_IC_DATA_OUT_A 77
#define GPO_SYS_IOMUX_U2_DW_UART_RTS_N 78
#define GPO_SYS_IOMUX_U2_DW_UART_SOUT 79
#define GPO_SYS_IOMUX_U2_SSP_SPI_SSPCLKOUT 80
#define GPO_SYS_IOMUX_U2_SSP_SPI_SSPFSSOUT 81
#define GPO_SYS_IOMUX_U2_SSP_SPI_SSPTXD 82
#define GPO_SYS_IOMUX_U3_DW_I2C_IC_CLK_OUT_A 83
#define GPO_SYS_IOMUX_U3_DW_I2C_IC_DATA_OUT_A 84
#define GPO_SYS_IOMUX_U3_DW_UART_SOUT 85
#define GPO_SYS_IOMUX_U3_SSP_SPI_SSPCLKOUT 86
#define GPO_SYS_IOMUX_U3_SSP_SPI_SSPFSSOUT 87
#define GPO_SYS_IOMUX_U3_SSP_SPI_SSPTXD 88
#define GPO_SYS_IOMUX_U4_DW_I2C_IC_CLK_OUT_A 89
#define GPO_SYS_IOMUX_U4_DW_I2C_IC_DATA_OUT_A 90
#define GPO_SYS_IOMUX_U4_DW_UART_RTS_N 91
#define GPO_SYS_IOMUX_U4_DW_UART_SOUT 92
```


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```
#define GPO_SYS_IOMUX_U4_SSP_SPI_SSPCLKOUT 93
#define GPO_SYS_IOMUX_U4_SSP_SPI_SSPFSSOUT 94
#define GPO_SYS_IOMUX_U4_SSP_SPI_SSPTXD 95
#define GPO_SYS_IOMUX_U5_DW_I2C_IC_CLK_OUT_A 96
#define GPO_SYS_IOMUX_U5_DW_I2C_IC_DATA_OUT_A 97
#define GPO_SYS_IOMUX_U5_DW_UART_RTS_N 98
#define GPO_SYS_IOMUX_U5_DW_UART_SOUT 99
#define GPO_SYS_IOMUX_U5_SSP_SPI_SSPCLKOUT 100
#define GPO_SYS_IOMUX_U5_SSP_SPI_SSPFSSOUT 101
#define GPO_SYS_IOMUX_U5_SSP_SPI_SSPTXD 102
#define GPO_SYS_IOMUX_U6_DW_I2C_IC_CLK_OUT_A 103
#define GPO_SYS_IOMUX_U6_DW_I2C_IC_DATA_OUT_A 104
#define GPO_SYS_IOMUX_U6_SSP_SPI_SSPCLKOUT 105
#define GPO_SYS_IOMUX_U6_SSP_SPI_SSPFSSOUT 106
#define GPO_SYS_IOMUX_U6_SSP_SPI_SSPTXD 107

//GPEN SYS_IOMUX
#define GPEN_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_CEC_SDA_OEN 2
#define GPEN_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SCL_OEN 3
#define GPEN_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SDA_OEN 4
#define GPEN_SYS_IOMUX_U0_DW_I2C_IC_CLK_OE 5
#define GPEN_SYS_IOMUX_U0_DW_I2C_IC_DATA_OE 6
#define GPEN_SYS_IOMUX_U0_HIFI4_JTDOEN 7
#define GPEN_SYS_IOMUX_U0_JTAG_CERTIFICATION_TDO_OE 8
#define GPEN_SYS_IOMUX_U0_PWM_8CH_PTC_OE_N_0 9
#define GPEN_SYS_IOMUX_U0_PWM_8CH_PTC_OE_N_1 10
#define GPEN_SYS_IOMUX_U0_PWM_8CH_PTC_OE_N_2 11
#define GPEN_SYS_IOMUX_U0_PWM_8CH_PTC_OE_N_3 12
#define GPEN_SYS_IOMUX_U0_SSP_SPI_NSSPCTLOE 13
#define GPEN_SYS_IOMUX_U0_SSP_SPI_NSSPOE 14
#define GPEN_SYS_IOMUX_U0_TDM16SLOT_NPCM_SYNCOE 15
#define GPEN_SYS_IOMUX_U0_TDM16SLOT_NPCM_TXDOE 16
#define GPEN_SYS_IOMUX_U1_DW_I2C_IC_CLK_OE 17
#define GPEN_SYS_IOMUX_U1_DW_I2C_IC_DATA_OE 18
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CCMD_OUT_EN 19
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_0 20
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_1 21
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_2 22
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_3 23
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_4 24
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_5 25
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_6 26
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_7 27
#define GPEN_SYS_IOMUX_U1_SSP_SPI_NSSPCTLOE 28
#define GPEN_SYS_IOMUX_U1_SSP_SPI_NSSPOE 29
#define GPEN_SYS_IOMUX_U2_DW_I2C_IC_CLK_OE 30
#define GPEN_SYS_IOMUX_U2_DW_I2C_IC_DATA_OE 31
#define GPEN_SYS_IOMUX_U2_SSP_SPI_NSSPCTLOE 32
#define GPEN_SYS_IOMUX_U2_SSP_SPI_NSSPOE 33
#define GPEN_SYS_IOMUX_U3_DW_I2C_IC_CLK_OE 34
#define GPEN_SYS_IOMUX_U3_DW_I2C_IC_DATA_OE 35
#define GPEN_SYS_IOMUX_U3_SSP_SPI_NSSPCTLOE 36
#define GPEN_SYS_IOMUX_U3_SSP_SPI_NSSPOE 37
#define GPEN_SYS_IOMUX_U4_DW_I2C_IC_CLK_OE 38
#define GPEN_SYS_IOMUX_U4_DW_I2C_IC_DATA_OE 39
#define GPEN_SYS_IOMUX_U4_SSP_SPI_NSSPCTLOE 40
#define GPEN_SYS_IOMUX_U4_SSP_SPI_NSSPOE 41
#define GPEN_SYS_IOMUX_U5_DW_I2C_IC_CLK_OE 42
#define GPEN_SYS_IOMUX_U5_DW_I2C_IC_DATA_OE 43
#define GPEN_SYS_IOMUX_U5_SSP_SPI_NSSPCTLOE 44
#define GPEN_SYS_IOMUX_U5_SSP_SPI_NSSPOE 45
#define GPEN_SYS_IOMUX_U6_DW_I2C_IC_CLK_OE 46
#define GPEN_SYS_IOMUX_U6_DW_I2C_IC_DATA_OE 47
#define GPEN_SYS_IOMUX_U6_SSP_SPI_NSSPCTLOE 48
#define GPEN_SYS_IOMUX_U6_SSP_SPI_NSSPOE 49

//GPI SYS_IOMUX
#define GPI_SYS_IOMUX_U0_WAVE511_I_UART_RXSIN 0
#define GPI_SYS_IOMUX_U0_CAN_CTRL_RXD 1
#define GPI_SYS_IOMUX_U0_CDN_USB_OVERCURRENT_N_IO 2
#define GPI_SYS_IOMUX_U0_CDNS_SPDIF_SPDIFI 3
#define GPI_SYS_IOMUX_U0_CLKRST_SRC_BYPASS_JTAG_TRSTN 4
```


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```
#define GPI_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_CEC_SDA_IN 5
#define GPI_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SCL_IN 6
#define GPI_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SDA_IN 7
#define GPI_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_HPD 8
#define GPI_SYS_IOMUX_U0_DW_I2C_IC_CLK_IN_A 9
#define GPI_SYS_IOMUX_U0_DW_I2C_IC_DATA_IN_A 10
#define GPI_SYS_IOMUX_U0_DW_SDIO_CARD_DETECT_N 11
#define GPI_SYS_IOMUX_U0_DW_SDIO_CARD_INT_N 12
#define GPI_SYS_IOMUX_U0_DW_SDIO_CARD_WRITE_PRT 13
#define GPI_SYS_IOMUX_U0_DW_UART_SIN 14
#define GPI_SYS_IOMUX_U0_HIFI4_JTCK 15
#define GPI_SYS_IOMUX_U0_HIFI4_JTDI 16
#define GPI_SYS_IOMUX_U0_HIFI4_JTMS 17
#define GPI_SYS_IOMUX_U0_HIFI4_JTRSTN 18
#define GPI_SYS_IOMUX_U0_JTAG_CERTIFICATION_TDI 19
#define GPI_SYS_IOMUX_U0_JTAG_CERTIFICATION_TMS 20
#define GPI_SYS_IOMUX_U0_PDM_4MIC_DMIC0_DIN 21
#define GPI_SYS_IOMUX_U0_PDM_4MIC_DMIC1_DIN 22
#define GPI_SYS_IOMUX_U0_SAIF_AUDIO_SDIN_MUX_I2SRX_EXT_SDIN0 23
#define GPI_SYS_IOMUX_U0_SAIF_AUDIO_SDIN_MUX_I2SRX_EXT_SDIN1 24
#define GPI_SYS_IOMUX_U0_SAIF_AUDIO_SDIN_MUX_I2SRX_EXT_SDIN2 25
#define GPI_SYS_IOMUX_U0_SSP_SPI_SSPCLKIN 26
#define GPI_SYS_IOMUX_U0_SSP_SPI_SSPFSSIN 27
#define GPI_SYS_IOMUX_U0_SSP_SPI_SSPRXD 28
#define GPI_SYS_IOMUX_U0_SYS_CRG_CLK_JTAG_TCK 29
#define GPI_SYS_IOMUX_U0_SYS_CRG_EXT_MCLK 30
#define GPI_SYS_IOMUX_U0_SYS_CRG_I2SRX_BCLK_SLV 31
#define GPI_SYS_IOMUX_U0_SYS_CRG_I2SRX_LRCK_SLV 32
#define GPI_SYS_IOMUX_U0_SYS_CRG_I2STX_BCLK_SLV 33
#define GPI_SYS_IOMUX_U0_SYS_CRG_I2STX_LRCK_SLV 34
#define GPI_SYS_IOMUX_U0_SYS_CRG_TDM_CLK_SLV 35
#define GPI_SYS_IOMUX_U0_TDM16SLOT_PCM_RXD 36
#define GPI_SYS_IOMUX_U0_TDM16SLOT_PCM_SYNCIN 37
#define GPI_SYS_IOMUX_U1_CAN_CTRL_RXD 38
#define GPI_SYS_IOMUX_U1_DW_I2C_IC_CLK_IN_A 39
#define GPI_SYS_IOMUX_U1_DW_I2C_IC_DATA_IN_A 40
#define GPI_SYS_IOMUX_U1_DW_SDIO_CARD_DETECT_N 41
#define GPI_SYS_IOMUX_U1_DW_SDIO_CARD_INT_N 42
#define GPI_SYS_IOMUX_U1_DW_SDIO_CARD_WRITE_PRT 43
#define GPI_SYS_IOMUX_U1_DW_SDIO_CCMD_IN 44
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_0 45
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_1 46
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_2 47
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_3 48
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_4 49
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_5 50
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_6 51
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_7 52
#define GPI_SYS_IOMUX_U1_DW_SDIO_DATA_STROBE 53
#define GPI_SYS_IOMUX_U1_DW_UART_CTS_N 54
#define GPI_SYS_IOMUX_U1_DW_UART_SIN 55
#define GPI_SYS_IOMUX_U1_SSP_SPI_SSPCLKIN 56
#define GPI_SYS_IOMUX_U1_SSP_SPI_SSPFSSIN 57
#define GPI_SYS_IOMUX_U1_SSP_SPI_SSPRXD 58
#define GPI_SYS_IOMUX_U2_DW_I2C_IC_CLK_IN_A 59
#define GPI_SYS_IOMUX_U2_DW_I2C_IC_DATA_IN_A 60
#define GPI_SYS_IOMUX_U2_DW_UART_CTS_N 61
#define GPI_SYS_IOMUX_U2_DW_UART_SIN 62
#define GPI_SYS_IOMUX_U2_SSP_SPI_SSPCLKIN 63
#define GPI_SYS_IOMUX_U2_SSP_SPI_SSPFSSIN 64
#define GPI_SYS_IOMUX_U2_SSP_SPI_SSPRXD 65
#define GPI_SYS_IOMUX_U3_DW_I2C_IC_CLK_IN_A 66
#define GPI_SYS_IOMUX_U3_DW_I2C_IC_DATA_IN_A 67
#define GPI_SYS_IOMUX_U3_DW_UART_SIN 68
#define GPI_SYS_IOMUX_U3_SSP_SPI_SSPCLKIN 69
#define GPI_SYS_IOMUX_U3_SSP_SPI_SSPFSSIN 70
#define GPI_SYS_IOMUX_U3_SSP_SPI_SSPRXD 71
#define GPI_SYS_IOMUX_U4_DW_I2C_IC_CLK_IN_A 72
#define GPI_SYS_IOMUX_U4_DW_I2C_IC_DATA_IN_A 73
#define GPI_SYS_IOMUX_U4_DW_UART_CTS_N 74
#define GPI_SYS_IOMUX_U4_DW_UART_SIN 75
#define GPI_SYS_IOMUX_U4_SSP_SPI_SSPCLKIN 76
```


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```
#define GPI_SYS_IOMUX_U4_SSP_SPI_SSPFSSIN 77
#define GPI_SYS_IOMUX_U4_SSP_SPI_SSPRXD 78
#define GPI_SYS_IOMUX_U5_DW_I2C_IC_CLK_IN_A 79
#define GPI_SYS_IOMUX_U5_DW_I2C_IC_DATA_IN_A 80
#define GPI_SYS_IOMUX_U5_DW_UART_CTS_N 81
#define GPI_SYS_IOMUX_U5_DW_UART_SIN 82
#define GPI_SYS_IOMUX_U5_SSP_SPI_SSPCLKIN 83
#define GPI_SYS_IOMUX_U5_SSP_SPI_SSPFSSIN 84
#define GPI_SYS_IOMUX_U5_SSP_SPI_SSPRXD 85
#define GPI_SYS_IOMUX_U6_DW_I2C_IC_CLK_IN_A 86
#define GPI_SYS_IOMUX_U6_DW_I2C_IC_DATA_IN_A 87
#define GPI_SYS_IOMUX_U6_SSP_SPI_SSPCLKIN 88
#define GPI_SYS_IOMUX_U6_SSP_SPI_SSPFSSIN 89
#define GPI_SYS_IOMUX_U6_SSP_SPI_SSPRXD 90

//GPO AON_IOMUX
#define GPO_AON_IOMUX_U0_AON_CRG_CLK_32K_OUT 2
#define GPO_AON_IOMUX_U0_PWM_8CH_PTC_PWM_4 3
#define GPO_AON_IOMUX_U0_PWM_8CH_PTC_PWM_5 4
#define GPO_AON_IOMUX_U0_PWM_8CH_PTC_PWM_6 5
#define GPO_AON_IOMUX_U0_PWM_8CH_PTC_PWM_7 6
#define GPO_AON_IOMUX_U0_SYS_CRG_CLK_GCLK0 7
#define GPO_AON_IOMUX_U0_SYS_CRG_CLK_GCLK1 8
#define GPO_AON_IOMUX_U0_SYS_CRG_CLK_GCLK2 9

//GPEN AON_IOMUX
#define GPEN_AON_IOMUX_U0_PWM_8CH_PTC_OE_N_4 2
#define GPEN_AON_IOMUX_U0_PWM_8CH_PTC_OE_N_5 3
#define GPEN_AON_IOMUX_U0_PWM_8CH_PTC_OE_N_6 4
#define GPEN_AON_IOMUX_U0_PWM_8CH_PTC_OE_N_7 5

//GPI AON_IOMUX
#define GPI_AON_IOMUX_U0_PMU_IO_EVENT_STUB_GPIO_WAKEUP_0 0
#define GPI_AON_IOMUX_U0_PMU_IO_EVENT_STUB_GPIO_WAKEUP_1 1
#define GPI_AON_IOMUX_U0_PMU_IO_EVENT_STUB_GPIO_WAKEUP_2 2
#define GPI_AON_IOMUX_U0_PMU_IO_EVENT_STUB_GPIO_WAKEUP_3 3
```

2.7.6.5. Signal Index Table

The following code block shows the signal index of the JH-7110 GPIO ports.

Note:
Signal with prefix SYS_IOMUX is for GPIO use only, and signal with prefix AON_IOMUX is for RGPIO use only.

```
//GPO SYS_IOMUX
#define GPO_SYS_IOMUX_U0_WAVE511_O_UART_TXSOUT 2
#define GPO_SYS_IOMUX_U0_CAN_CTRL_STBY 3
#define GPO_SYS_IOMUX_U0_CAN_CTRL_TST_NEXT_BIT 4
#define GPO_SYS_IOMUX_U0_CAN_CTRL_TST_SAMPLE_POINT 5
#define GPO_SYS_IOMUX_U0_CAN_CTRL_TXD 6
#define GPO_SYS_IOMUX_U0_CDN_USB_DRIVE_VBUS_IO 7
#define GPO_SYS_IOMUX_U0_CDNS_QSPI_CSN1 8
#define GPO_SYS_IOMUX_U0_CDNS_SPDIF_SPDIFO 9
#define GPO_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_CEC_SDA_OUT 10
#define GPO_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SCL_OUT 11
#define GPO_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SDA_OUT 12
#define GPO_SYS_IOMUX_U0_DSKIT_WDT_WDOGRES 13
#define GPO_SYS_IOMUX_U0_DW_I2C_IC_CLK_OUT_A 14
#define GPO_SYS_IOMUX_U0_DW_I2C_IC_DATA_OUT_A 15
#define GPO_SYS_IOMUX_U0_DW_SDIO_BACK_END_POWER 16
#define GPO_SYS_IOMUX_U0_DW_SDIO_CARD_POWER_EN 17
#define GPO_SYS_IOMUX_U0_DW_SDIO_CCMD_OD_PULLUP_EN_N 18
#define GPO_SYS_IOMUX_U0_DW_SDIO_RST_N 19
#define GPO_SYS_IOMUX_U0_DW_UART_SOUT 20
#define GPO_SYS_IOMUX_U0_HIFI4_JTDO 21
#define GPO_SYS_IOMUX_U0_JTAG_CERTIFICATION_TDO 22
#define GPO_SYS_IOMUX_U0_PDM_4MIC_DMIC_MCLK 23
#define GPO_SYS_IOMUX_U0_PWM_8CH_PTC_PWM_0 24
```


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```
#define GPO_SYS_IOMUX_U0_PWM_8CH_PTC_PWM_1 25
#define GPO_SYS_IOMUX_U0_PWM_8CH_PTC_PWM_2 26
#define GPO_SYS_IOMUX_U0_PWM_8CH_PTC_PWM_3 27
#define GPO_SYS_IOMUX_U0_PWMDAC_PWMDAC_LEFT_OUTPUT 28
#define GPO_SYS_IOMUX_U0_PWMDAC_PWMDAC_RIGHT_OUTPUT 29
#define GPO_SYS_IOMUX_U0_SSP_SPI_SSPCLKOUT 30
#define GPO_SYS_IOMUX_U0_SSP_SPI_SSPFSSOUT 31
#define GPO_SYS_IOMUX_U0_SSP_SPI_SSPTXD 32
#define GPO_SYS_IOMUX_U0_SYS_CRG_CLK_GMAC_PHY 33
#define GPO_SYS_IOMUX_U0_SYS_CRG_I2SRX_BCLK_MST 34
#define GPO_SYS_IOMUX_U0_SYS_CRG_I2SRX_LRCK_MST 35
#define GPO_SYS_IOMUX_U0_SYS_CRG_I2STX_BCLK_MST 36
#define GPO_SYS_IOMUX_U0_SYS_CRG_I2STX_LRCK_MST 37
#define GPO_SYS_IOMUX_U0_SYS_CRG_MCLK_OUT 38
#define GPO_SYS_IOMUX_U0_SYS_CRG_TDM_CLK_MST 39
#define GPO_SYS_IOMUX_U0_TDM16SLOT_PCM_SYNCOUT 40
#define GPO_SYS_IOMUX_U0_TDM16SLOT_PCM_TXD 41
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TDATA_0 42
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TDATA_1 43
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TDATA_2 44
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TDATA_3 45
#define GPO_SYS_IOMUX_U0_U7MC_SFT7110_TRACE_COM_PIB_TREF 46
#define GPO_SYS_IOMUX_U1_CAN_CTRL_STBY 47
#define GPO_SYS_IOMUX_U1_CAN_CTRL_TST_NEXT_BIT 48
#define GPO_SYS_IOMUX_U1_CAN_CTRL_TST_SAMPLE_POINT 49
#define GPO_SYS_IOMUX_U1_CAN_CTRL_TXD 50
#define GPO_SYS_IOMUX_U1_DW_I2C_IC_CLK_OUT_A 51
#define GPO_SYS_IOMUX_U1_DW_I2C_IC_DATA_OUT_A 52
#define GPO_SYS_IOMUX_U1_DW_SDIO_BACK_END_POWER 53
#define GPO_SYS_IOMUX_U1_DW_SDIO_CARD_POWER_EN 54
#define GPO_SYS_IOMUX_U1_DW_SDIO_CCLK_OUT 55
#define GPO_SYS_IOMUX_U1_DW_SDIO_CCMD_OD_PULLUP_EN_N 56
#define GPO_SYS_IOMUX_U1_DW_SDIO_CCMD_OUT 57
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_0 58
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_1 59
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_2 60
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_3 61
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_4 62
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_5 63
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_6 64
#define GPO_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_7 65
#define GPO_SYS_IOMUX_U1_DW_SDIO_RST_N 66
#define GPO_SYS_IOMUX_U1_DW_UART_RTS_N 67
#define GPO_SYS_IOMUX_U1_DW_UART_SOUT 68
#define GPO_SYS_IOMUX_U1_I2STX_4CH_SDO0 69
#define GPO_SYS_IOMUX_U1_I2STX_4CH_SDO1 70
#define GPO_SYS_IOMUX_U1_I2STX_4CH_SDO2 71
#define GPO_SYS_IOMUX_U1_I2STX_4CH_SDO3 72
#define GPO_SYS_IOMUX_U1_SSP_SPI_SSPCLKOUT 73
#define GPO_SYS_IOMUX_U1_SSP_SPI_SSPFSSOUT 74
#define GPO_SYS_IOMUX_U1_SSP_SPI_SSPTXD 75
#define GPO_SYS_IOMUX_U2_DW_I2C_IC_CLK_OUT_A 76
#define GPO_SYS_IOMUX_U2_DW_I2C_IC_DATA_OUT_A 77
#define GPO_SYS_IOMUX_U2_DW_UART_RTS_N 78
#define GPO_SYS_IOMUX_U2_DW_UART_SOUT 79
#define GPO_SYS_IOMUX_U2_SSP_SPI_SSPCLKOUT 80
#define GPO_SYS_IOMUX_U2_SSP_SPI_SSPFSSOUT 81
#define GPO_SYS_IOMUX_U2_SSP_SPI_SSPTXD 82
#define GPO_SYS_IOMUX_U3_DW_I2C_IC_CLK_OUT_A 83
#define GPO_SYS_IOMUX_U3_DW_I2C_IC_DATA_OUT_A 84
#define GPO_SYS_IOMUX_U3_DW_UART_SOUT 85
#define GPO_SYS_IOMUX_U3_SSP_SPI_SSPCLKOUT 86
#define GPO_SYS_IOMUX_U3_SSP_SPI_SSPFSSOUT 87
#define GPO_SYS_IOMUX_U3_SSP_SPI_SSPTXD 88
#define GPO_SYS_IOMUX_U4_DW_I2C_IC_CLK_OUT_A 89
#define GPO_SYS_IOMUX_U4_DW_I2C_IC_DATA_OUT_A 90
#define GPO_SYS_IOMUX_U4_DW_UART_RTS_N 91
#define GPO_SYS_IOMUX_U4_DW_UART_SOUT 92
#define GPO_SYS_IOMUX_U4_SSP_SPI_SSPCLKOUT 93
#define GPO_SYS_IOMUX_U4_SSP_SPI_SSPFSSOUT 94
#define GPO_SYS_IOMUX_U4_SSP_SPI_SSPTXD 95
#define GPO_SYS_IOMUX_U5_DW_I2C_IC_CLK_OUT_A 96
```


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```
#define GPO_SYS_IOMUX_U5_DW_I2C_IC_DATA_OUT_A 97
#define GPO_SYS_IOMUX_U5_DW_UART_RTS_N 98
#define GPO_SYS_IOMUX_U5_DW_UART_SOUT 99
#define GPO_SYS_IOMUX_U5_SSP_SPI_SSPCLKOUT 100
#define GPO_SYS_IOMUX_U5_SSP_SPI_SSPFSSOUT 101
#define GPO_SYS_IOMUX_U5_SSP_SPI_SSPTXD 102
#define GPO_SYS_IOMUX_U6_DW_I2C_IC_CLK_OUT_A 103
#define GPO_SYS_IOMUX_U6_DW_I2C_IC_DATA_OUT_A 104
#define GPO_SYS_IOMUX_U6_SSP_SPI_SSPCLKOUT 105
#define GPO_SYS_IOMUX_U6_SSP_SPI_SSPFSSOUT 106
#define GPO_SYS_IOMUX_U6_SSP_SPI_SSPTXD 107

//GPEN SYS_IOMUX
#define GPEN_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_CEC_SDA_OEN 2
#define GPEN_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SCL_OEN 3
#define GPEN_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SDA_OEN 4
#define GPEN_SYS_IOMUX_U0_DW_I2C_IC_CLK_OE 5
#define GPEN_SYS_IOMUX_U0_DW_I2C_IC_DATA_OE 6
#define GPEN_SYS_IOMUX_U0_HIFI4_JTDOEN 7
#define GPEN_SYS_IOMUX_U0_JTAG_CERTIFICATION_TDO_OE 8
#define GPEN_SYS_IOMUX_U0_PWM_8CH_PTC_OE_N_0 9
#define GPEN_SYS_IOMUX_U0_PWM_8CH_PTC_OE_N_1 10
#define GPEN_SYS_IOMUX_U0_PWM_8CH_PTC_OE_N_2 11
#define GPEN_SYS_IOMUX_U0_PWM_8CH_PTC_OE_N_3 12
#define GPEN_SYS_IOMUX_U0_SSP_SPI_NSSPCTLOE 13
#define GPEN_SYS_IOMUX_U0_SSP_SPI_NSSPOE 14
#define GPEN_SYS_IOMUX_U0_TDM16SLOT_NPCM_SYNCOE 15
#define GPEN_SYS_IOMUX_U0_TDM16SLOT_NPCM_TXDOE 16
#define GPEN_SYS_IOMUX_U1_DW_I2C_IC_CLK_OE 17
#define GPEN_SYS_IOMUX_U1_DW_I2C_IC_DATA_OE 18
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CCMD_OUT_EN 19
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_0 20
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_1 21
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_2 22
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_3 23
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_4 24
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_5 25
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_6 26
#define GPEN_SYS_IOMUX_U1_DW_SDIO_CDATA_OUT_EN_7 27
#define GPEN_SYS_IOMUX_U1_SSP_SPI_NSSPCTLOE 28
#define GPEN_SYS_IOMUX_U1_SSP_SPI_NSSPOE 29
#define GPEN_SYS_IOMUX_U2_DW_I2C_IC_CLK_OE 30
#define GPEN_SYS_IOMUX_U2_DW_I2C_IC_DATA_OE 31
#define GPEN_SYS_IOMUX_U2_SSP_SPI_NSSPCTLOE 32
#define GPEN_SYS_IOMUX_U2_SSP_SPI_NSSPOE 33
#define GPEN_SYS_IOMUX_U3_DW_I2C_IC_CLK_OE 34
#define GPEN_SYS_IOMUX_U3_DW_I2C_IC_DATA_OE 35
#define GPEN_SYS_IOMUX_U3_SSP_SPI_NSSPCTLOE 36
#define GPEN_SYS_IOMUX_U3_SSP_SPI_NSSPOE 37
#define GPEN_SYS_IOMUX_U4_DW_I2C_IC_CLK_OE 38
#define GPEN_SYS_IOMUX_U4_DW_I2C_IC_DATA_OE 39
#define GPEN_SYS_IOMUX_U4_SSP_SPI_NSSPCTLOE 40
#define GPEN_SYS_IOMUX_U4_SSP_SPI_NSSPOE 41
#define GPEN_SYS_IOMUX_U5_DW_I2C_IC_CLK_OE 42
#define GPEN_SYS_IOMUX_U5_DW_I2C_IC_DATA_OE 43
#define GPEN_SYS_IOMUX_U5_SSP_SPI_NSSPCTLOE 44
#define GPEN_SYS_IOMUX_U5_SSP_SPI_NSSPOE 45
#define GPEN_SYS_IOMUX_U6_DW_I2C_IC_CLK_OE 46
#define GPEN_SYS_IOMUX_U6_DW_I2C_IC_DATA_OE 47
#define GPEN_SYS_IOMUX_U6_SSP_SPI_NSSPCTLOE 48
#define GPEN_SYS_IOMUX_U6_SSP_SPI_NSSPOE 49

//GPI SYS_IOMUX
#define GPI_SYS_IOMUX_U0_WAVE511_I_UART_RXSIN 0
#define GPI_SYS_IOMUX_U0_CAN_CTRL_RXD 1
#define GPI_SYS_IOMUX_U0_CDN_USB_OVERCURRENT_N_IO 2
#define GPI_SYS_IOMUX_U0_CDNS_SPDIF_SPDIFI 3
#define GPI_SYS_IOMUX_U0_CLKRST_SRC_BYPASS_JTAG_TRSTN 4
#define GPI_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_CEC_SDA_IN 5
#define GPI_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SCL_IN 6
#define GPI_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_DDC_SDA_IN 7
#define GPI_SYS_IOMUX_U0_DOM_VOUT_TOP_U0_HDMI_TX_PIN_HPD 8
```


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```
#define GPI_SYS_IOMUX_U0_DW_I2C_IC_CLK_IN_A 9
#define GPI_SYS_IOMUX_U0_DW_I2C_IC_DATA_IN_A 10
#define GPI_SYS_IOMUX_U0_DW_SDIO_CARD_DETECT_N 11
#define GPI_SYS_IOMUX_U0_DW_SDIO_CARD_INT_N 12
#define GPI_SYS_IOMUX_U0_DW_SDIO_CARD_WRITE_PRT 13
#define GPI_SYS_IOMUX_U0_DW_UART_SIN 14
#define GPI_SYS_IOMUX_U0_HIFI4_JTCK 15
#define GPI_SYS_IOMUX_U0_HIFI4_JTDI 16
#define GPI_SYS_IOMUX_U0_HIFI4_JTMS 17
#define GPI_SYS_IOMUX_U0_HIFI4_JTRSTN 18
#define GPI_SYS_IOMUX_U0_JTAG_CERTIFICATION_TDI 19
#define GPI_SYS_IOMUX_U0_JTAG_CERTIFICATION_TMS 20
#define GPI_SYS_IOMUX_U0_PDM_4MIC_DMIC0_DIN 21
#define GPI_SYS_IOMUX_U0_PDM_4MIC_DMIC1_DIN 22
#define GPI_SYS_IOMUX_U0_SAIF_AUDIO_SDIN_MUX_I2SRX_EXT_SDIN0 23
#define GPI_SYS_IOMUX_U0_SAIF_AUDIO_SDIN_MUX_I2SRX_EXT_SDIN1 24
#define GPI_SYS_IOMUX_U0_SAIF_AUDIO_SDIN_MUX_I2SRX_EXT_SDIN2 25
#define GPI_SYS_IOMUX_U0_SSP_SPI_SSPCLKIN 26
#define GPI_SYS_IOMUX_U0_SSP_SPI_SSPFSSIN 27
#define GPI_SYS_IOMUX_U0_SSP_SPI_SSPRXD 28
#define GPI_SYS_IOMUX_U0_SYS_CRG_CLK_JTAG_TCK 29
#define GPI_SYS_IOMUX_U0_SYS_CRG_EXT_MCLK 30
#define GPI_SYS_IOMUX_U0_SYS_CRG_I2SRX_BCLK_SLV 31
#define GPI_SYS_IOMUX_U0_SYS_CRG_I2SRX_LRCK_SLV 32
#define GPI_SYS_IOMUX_U0_SYS_CRG_I2STX_BCLK_SLV 33
#define GPI_SYS_IOMUX_U0_SYS_CRG_I2STX_LRCK_SLV 34
#define GPI_SYS_IOMUX_U0_SYS_CRG_TDM_CLK_SLV 35
#define GPI_SYS_IOMUX_U0_TDM16SLOT_PCM_RXD 36
#define GPI_SYS_IOMUX_U0_TDM16SLOT_PCM_SYNCIN 37
#define GPI_SYS_IOMUX_U1_CAN_CTRL_RXD 38
#define GPI_SYS_IOMUX_U1_DW_I2C_IC_CLK_IN_A 39
#define GPI_SYS_IOMUX_U1_DW_I2C_IC_DATA_IN_A 40
#define GPI_SYS_IOMUX_U1_DW_SDIO_CARD_DETECT_N 41
#define GPI_SYS_IOMUX_U1_DW_SDIO_CARD_INT_N 42
#define GPI_SYS_IOMUX_U1_DW_SDIO_CARD_WRITE_PRT 43
#define GPI_SYS_IOMUX_U1_DW_SDIO_CCMD_IN 44
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_0 45
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_1 46
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_2 47
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_3 48
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_4 49
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_5 50
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_6 51
#define GPI_SYS_IOMUX_U1_DW_SDIO_CDATA_IN_7 52
#define GPI_SYS_IOMUX_U1_DW_SDIO_DATA_STROBE 53
#define GPI_SYS_IOMUX_U1_DW_UART_CTS_N 54
#define GPI_SYS_IOMUX_U1_DW_UART_SIN 55
#define GPI_SYS_IOMUX_U1_SSP_SPI_SSPCLKIN 56
#define GPI_SYS_IOMUX_U1_SSP_SPI_SSPFSSIN 57
#define GPI_SYS_IOMUX_U1_SSP_SPI_SSPRXD 58
#define GPI_SYS_IOMUX_U2_DW_I2C_IC_CLK_IN_A 59
#define GPI_SYS_IOMUX_U2_DW_I2C_IC_DATA_IN_A 60
#define GPI_SYS_IOMUX_U2_DW_UART_CTS_N 61
#define GPI_SYS_IOMUX_U2_DW_UART_SIN 62
#define GPI_SYS_IOMUX_U2_SSP_SPI_SSPCLKIN 63
#define GPI_SYS_IOMUX_U2_SSP_SPI_SSPFSSIN 64
#define GPI_SYS_IOMUX_U2_SSP_SPI_SSPRXD 65
#define GPI_SYS_IOMUX_U3_DW_I2C_IC_CLK_IN_A 66
#define GPI_SYS_IOMUX_U3_DW_I2C_IC_DATA_IN_A 67
#define GPI_SYS_IOMUX_U3_DW_UART_SIN 68
#define GPI_SYS_IOMUX_U3_SSP_SPI_SSPCLKIN 69
#define GPI_SYS_IOMUX_U3_SSP_SPI_SSPFSSIN 70
#define GPI_SYS_IOMUX_U3_SSP_SPI_SSPRXD 71
#define GPI_SYS_IOMUX_U4_DW_I2C_IC_CLK_IN_A 72
#define GPI_SYS_IOMUX_U4_DW_I2C_IC_DATA_IN_A 73
#define GPI_SYS_IOMUX_U4_DW_UART_CTS_N 74
#define GPI_SYS_IOMUX_U4_DW_UART_SIN 75
#define GPI_SYS_IOMUX_U4_SSP_SPI_SSPCLKIN 76
#define GPI_SYS_IOMUX_U4_SSP_SPI_SSPFSSIN 77
#define GPI_SYS_IOMUX_U4_SSP_SPI_SSPRXD 78
#define GPI_SYS_IOMUX_U5_DW_I2C_IC_CLK_IN_A 79
#define GPI_SYS_IOMUX_U5_DW_I2C_IC_DATA_IN_A 80
```


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```
#define GPI_SYS_IOMUX_U5_DW_UART_CTS_N 81
#define GPI_SYS_IOMUX_U5_DW_UART_SIN 82
#define GPI_SYS_IOMUX_U5_SSP_SPI_SSPCLKIN 83
#define GPI_SYS_IOMUX_U5_SSP_SPI_SSPFSSIN 84
#define GPI_SYS_IOMUX_U5_SSP_SPI_SSPRXD 85
#define GPI_SYS_IOMUX_U6_DW_I2C_IC_CLK_IN_A 86
#define GPI_SYS_IOMUX_U6_DW_I2C_IC_DATA_IN_A 87
#define GPI_SYS_IOMUX_U6_SSP_SPI_SSPCLKIN 88
#define GPI_SYS_IOMUX_U6_SSP_SPI_SSPFSSIN 89
#define GPI_SYS_IOMUX_U6_SSP_SPI_SSPRXD 90

//GPO AON_IOMUX
#define GPO_AON_IOMUX_U0_AON_CRG_CLK_32K_OUT 2
#define GPO_AON_IOMUX_U0_PWM_8CH_PTC_PWM_4 3
#define GPO_AON_IOMUX_U0_PWM_8CH_PTC_PWM_5 4
#define GPO_AON_IOMUX_U0_PWM_8CH_PTC_PWM_6 5
#define GPO_AON_IOMUX_U0_PWM_8CH_PTC_PWM_7 6
#define GPO_AON_IOMUX_U0_SYS_CRG_CLK_GCLK0 7
#define GPO_AON_IOMUX_U0_SYS_CRG_CLK_GCLK1 8
#define GPO_AON_IOMUX_U0_SYS_CRG_CLK_GCLK2 9

//GPEN AON_IOMUX
#define GPEN_AON_IOMUX_U0_PWM_8CH_PTC_OE_N_4 2
#define GPEN_AON_IOMUX_U0_PWM_8CH_PTC_OE_N_5 3
#define GPEN_AON_IOMUX_U0_PWM_8CH_PTC_OE_N_6 4
#define GPEN_AON_IOMUX_U0_PWM_8CH_PTC_OE_N_7 5

//GPI AON_IOMUX
#define GPI_AON_IOMUX_U0_PMU_IO_EVENT_STUB_GPIO_WAKEUP_0 0
#define GPI_AON_IOMUX_U0_PMU_IO_EVENT_STUB_GPIO_WAKEUP_1 1
#define GPI_AON_IOMUX_U0_PMU_IO_EVENT_STUB_GPIO_WAKEUP_2 2
#define GPI_AON_IOMUX_U0_PMU_IO_EVENT_STUB_GPIO_WAKEUP_3 3
```

2.7.7. GPIO Voltage Selection Registers

JH-7110 GPIO supports to select voltage between 1.8 V and 3.3 V.

You can use the following registers to set voltage.

SYS SYSCONSAIF SYSCFG 12

Table 2-46 SYS SYSCONSAIF SYSCFG 12 Register Description

Offset	**16'h0**			
Access	**RW**			
Bit	**Name**	**Access**	**Default**	**Description**
[31]	Reserved		0	Reserved
[3:0]	SYSCFG_gpio_sel18_cfg	WR	0x0	Set the GPIO voltage of all the 4 GPIO groups in this field: • Bit 0 = 0 : GPIO Group 0 (GPIO21-35) voltage select 3.3 V • Bit 0 = 1 : GPIO Group 0 (GPIO21-35) voltage select 1.8 V • Bit 1 = 0 : GPIO Group 1 (GPIO36-63) voltage select 3.3 V • Bit 1 = 1 : GPIO Group 1 (GPIO36-63) voltage select 1.38V • Bit 2 = 0 : GPIO Group 2 (GPIO0-6) voltage select 3.3 V

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Table 2-46 SYS SYSCONSAIF SYSCFG 12 Register Description (continued)

Offset	16'h0			
Access	RW			
Bit	Name	Access	Default	Description
				• Bit 2 = 1: GPIO Group 2 (GPIO0-6) voltage select 1.8 V • Bit 3 = 0 : GPIO Group 3 (GPIO7-20) voltage select 3.3 V • Bit 3 = 1 : GPIO Group 3 (GPIO7-20) voltage select 1.8 V
[31:4]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 596

Table 2-47 SYS IOMUX CFG SAIF SYSCFG 596 Register Description

Offset	0x254			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_RXD0_-syscon	WR	0x2	• [1:0] = 0 : GMAC1 IO voltage select 3.3 V • [1:0] = 1: GMAC1 IO voltage select 2.5 V • [1:0] = 2: GMAC1 IO voltage select 1.8 V
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 96

Table 2-48 AON IOMUX CFG SAIF SYSCFG 96 Register Description

Offset	0x60			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_RXD0_-syscon	WR	0x2	• [1:0] = 0 : GMAC0 IO voltage select 3.3 V • [1:0] = 1: GMAC0 IO voltage select 2.5 V • [1:0] = 2: GMAC0 IO voltage select 1.8 V
[2:31]	Reserved	None	0x0	Reserved

2.7.8. GPIO Voltage Selection IOs

JH-7110 GPIO supports to select voltage between 1.8 V and 3.3 V.

You can use the following IOs to set voltage.

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Table 2-49 GPIO Voltage Selection IOs

IO Signal	Description	Options
PAD_SD_SEL	Select voltage for SDIO0	The following values are available: • 0: 3.3 V • 1: 1.8 V
PAD_QSPI_SEL	Select voltage for QSPI	The following values are available: • 0: 3.3 V • 1: 1.8 V

2.8. System Control Registers

2.8.1. SYS CRG

The JH-7110 system provides the following SYS CRM system control registers.

Clock CPU Root

Table 2-50 Clock CPU Root Register Description

Offset	**16'h0**		
Access	**RW**		
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_osc • clk_pll0
[0:23]	Reserved	0	Reserved

Clock CPU Core

Table 2-51 Clock CPU Core Register Description

Offset	**16'h4**		
Access	**RW**		
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd1	Clock divider coefficient:

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Table 2-51 Clock CPU Core Register Description (continued)

Offset	16'h4		
Access	RW		
Bit	Name	Default	Description
			• Max: 7 • Default: 1 • Min: 1 • Typical: 1

Clock CPU Bus

Table 2-52 Clock CPU Bus Register Description

Offset	16'h8		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

Clock GPU Root

Table 2-53 Clock GPU Root Register Description

Offset	16'hc		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_pll2 • clk_pll1
[0:23]	Reserved	0	Reserved

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Clock Peripheral Root

Table 2-54 Clock Peripheral Root Register Description

Offset	16'h10		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_pll0 • clk_pll2
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

Clock Bus Root

Table 2-55 Clock Bus Root Register Description

Offset	16'h14		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_osc • clk_pll2
[0:23]	Reserved	0	Reserved

clk_nocstg_bus

Table 2-56 clk_nocstg_bus Register Description

Offset	16'h18		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved

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Table 2-56 clk_nocstg_bus Register Description (continued)

Offset	16'h18		
Access	RW		
Bit	Name	Default	Description
[0:23]	clk_divcfg	24'd3	Clock divider coefficient: • Max: 3 • Default: 3 • Min: 3 • Typical: 3

Clock AXI Configuration 0

Table 2-57 Clock AXI Configuration 0 Register Description

Offset	16'h1c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd3	Clock divider coefficient: • Max: 3 • Default: 3 • Min: 3 • Typical: 3

clk_stg_axiahb

Table 2-58 clk_stg_axiahb Register Description

Offset	16'h20		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

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Clock AHB 0

Table 2-59 Clock AHB 0 Register Description

Offset	16'h24		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock AHB 1

Table 2-60 Clock AHB 1 Register Description

Offset	16'h28		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock APB Bus Function

Table 2-61 Clock APB Bus Function Register Description

Offset	16'h2c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd4	Clock divider coefficient: • Max: 8 • Default: 4 • Min: 4 • Typical: 4

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Clock APB 0

Table 2-62 Clock APB 0 Register Description

Offset	16'h30		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock PLL 0 Divider 2

Table 2-63 Clock PLL 0 Divider 2 Register Description

Offset	16'h34		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

Clock PLL 1 Divider 2

Table 2-64 Clock PLL 1 Divider 2 Register Description

Offset	16'h38		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2

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Table 2-64 Clock PLL 1 Divider 2 Register Description (continued)

Offset	16'h38		
Access	RW		
Bit	Name	Default	Description
			• Min: 2 • Typical: 2

Clock PLL 2 Divider 2

Table 2-65 Clock PLL 2 Divider 2 Register Description

Offset	16'h3c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

Clock Audio Root

Table 2-66 Clock Audio Root Register Description

Offset	16'h40		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 8 • Default: 2 • Min: 2 • Typical: 2

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Clock MCLK Inner

Table 2-67 Clock MCLK Inner Register Description

Offset	16'h44		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd12	Clock divider coefficient: • Max: 64 • Default: 12 • Min: 12 • Typical: 12

Clock MCLK

Table 2-68 Clock MCLK Register Description

Offset	16'h48		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_mclk_inner • clk_mclk_ext
[0:23]	Reserved	0	Reserved

MCLK Out

Table 2-69 MCLK Out Register Description

Offset	16'h4c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock ISP 2x

Table 2-70 Clock ISP 2x Register Description

Offset	16'h50		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_pll2 • clk_pll1
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 8 • Default: 2 • Min: 2 • Typical: 2

Clock ISP AXI

Table 2-71 Clock ISP AXI Register Description

Offset	16'h54		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 4 • Default: 2 • Min: 2 • Typical: 2

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Clock GCLK 0

Table 2-72 Clock GCLK 0 Register Description

Offset	16'h58		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd20	Clock divider coefficient: • Max: 62 • Default: 20 • Min: 16 • Typical: 20

Clock GCLK 1

Table 2-73 Clock GCLK 1 Register Description

Offset	16'h5c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd16	Clock divider coefficient: • Max: 62 • Default: 16 • Min: 16 • Typical: 16

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Clock GCLK 2

Table 2-74 Clock GCLK 2 Register Description

Offset	16'h60		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd12	Clock divider coefficient: • Max: 62 • Default: 12 • Min: 12 • Typical: 12

U7MC Core Clock

Table 2-75 U7MC Core Clock Register Description

Offset	16'h64		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC Core Clock 1

Table 2-76 U7MC Core Clock 1 Register Description

Offset	16'h68		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved

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Table 2-76 U7MC Core Clock 1 Register Description (continued)

Offset	16'h68		
Access	RW		
Bit	Name	Default	Description
[0:23]	Reserved	0	Reserved

U7MC Core Clock 2

Table 2-77 U7MC Core Clock 2 Register Description

Offset	16'h6c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC Core Clock 3

Table 2-78 U7MC Core Clock 3 Register Description

Offset	16'h70		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC Core Clock 4

Table 2-79 U7MC Core Clock 4 Register Description

Offset	16'h74		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable

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Table 2-79 U7MC Core Clock 4 Register Description (continued)

Offset	16'h74		
Access	RW		
Bit	Name	Default	Description
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC Debug Clock

Table 2-80 U7MC Debug Clock Register Description

Offset	16'h78		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC RTC Toggle

Table 2-81 U7MC RTC Toggle Register Description

Offset	16'h7c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd6	Clock divider coefficient: • Max: 6 • Default: 6 • Min: 6 • Typical: 6

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U7MC Trace Clock 0

Table 2-82 U7MC Trace Clock 0 Register Description

Offset	16'h80		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC Trace Clock 1

Table 2-83 U7MC Trace Clock 1 Register Description

Offset	16'h84		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC Trace Clock 2

Table 2-84 U7MC Trace Clock 2 Register Description

Offset	16'h88		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U7MC Trace Clock 3

Table 2-85 U7MC Trace Clock 3 Register Description

Offset	16'h8c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC Trace Clock 4

Table 2-86 U7MC Trace Clock 4 Register Description

Offset	16'h90		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U7MC Trace COM Clock

Table 2-87 U7MC Trace COM Clock Register Description

Offset	16'h94		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_sft7110_noc_bus_clk_cpu_axi

Table 2-88 clk_u0_sft7110_noc_bus_clk_cpu_axi Register Description

Offset	16'h98		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_sft7110_noc_bus_clk_axicfg0_axi

Table 2-89 clk_u0_sft7110_noc_bus_clk_axicfg0_axi Register Description

Offset	16'h9c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_osc_div2

Table 2-90 clk_osc_div2 Register Description

Offset	16'ha0		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

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clk_pll1_div4

Table 2-91 clk_pll1_div4 Register Description

Offset	16'ha4		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

clk_pll1_div8

Table 2-92 clk_pll1_div8 Register Description

Offset	16'ha8		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

clk_ddr_bus

Table 2-93 clk_ddr_bus Register Description

Offset	16'hac		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector:

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Table 2-93 clk_ddr_bus Register Description (continued)

Offset	16'hac		
Access	RW		
Bit	Name	Default	Description
			• clk_osc_div2 • clk_pll1_div4 • clk_pll1_div8
[0:23]	Reserved	0	Reserved

clk_u0_ddr_sft7110_clk_axi

Table 2-94 clk_u0_ddr_sft7110_clk_axi Register Description

Offset	16'hb0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_gpu_core

Table 2-95 clk_gpu_core Register Description

Offset	16'hb4		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd3	Clock divider coefficient: • Max: 7 • Default: 3 • Min: 3 • Typical: 3

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clk_u0_img_gpu_core_clk

Table 2-96 clk_u0_img_gpu_core_clk Register Description

Offset	16'hb8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_img_gpu_sys_clk

Table 2-97 clk_u0_img_gpu_sys_clk Register Description

Offset	16'hbc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_img_gpu_clk_apb

Table 2-98 clk_u0_img_gpu_clk_apb Register Description

Offset	16'hc0		
Access	RW		
Bit	Name	Default	Description
31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_img_gpu_rtc_toggle

Table 2-99 clk_u0_img_gpu_rtc_toggle Register Description

Offset	16'hc4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd12	Clock divider coefficient: • Max: 12 • Default: 12 • Min: 12 • Typical: 12

clk_u0_sft7110_noc_bus_clk_gpu_axi

Table 2-100 clk_u0_sft7110_noc_bus_clk_gpu_axi Register Description

Offset	16'hc8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_dom_isp_top_clk_dom_isp_top_clk_ispcore_2x

Table 2-101 clk_u0_dom_isp_top_clk_dom_isp_top_clk_ispcore_2x Register Description

Offset	16'hcc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved

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Table 2-101 clk_u0_dom_isp_top_clk_dom_isp_top_clk_ispcore_2x Register Description (continued)

Offset	16'hcc		
Access	RW		
Bit	Name	Default	Description
[0:23]	Reserved	0	Reserved

clk_u0_dom_isp_top_clk_dom_isp_top_clk_isp_axi

Table 2-102 clk_u0_dom_isp_top_clk_dom_isp_top_clk_isp_axi Register Description

Offset	16'hd0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_sft7110_noc_bus_clk_isp_axi

Table 2-103 clk_u0_sft7110_noc_bus_clk_isp_axi Register Description

Offset	16'hd4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_hifi4_core

Table 2-104 clk_hifi4_core Register Description

Offset	16'hd8		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved

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Table 2-104 clk_hifi4_core Register Description (continued)

Offset	16'hd8		
Access	RW		
Bit	Name	Default	Description
[0:23]	clk_divcfg	24'd3	Clock divider coefficient: • Max: 15 • Default: 3 • Min: 3 • Typical: 3

clk_hifi4_axi

Table 2-105 clk_hifi4_axi Register Description

Offset	16'hdc		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

clk_u0_axi_cfg1_dec_clk_main

Table 2-106 clk_u0_axi_cfg1_dec_clk_main Register Description

Offset	16'he0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_axi_cfg1_dec_clk_ahb

Table 2-107 clk_u0_axi_cfg1_dec_clk_ahb Register Description

Offset	16'he4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_dom_vout_top_clk_dom_vout_top_clk_vout_src

Table 2-108 clk_u0_dom_vout_top_clk_dom_vout_top_clk_vout_src Register Description

Offset	16'he8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Video Output AXI

Table 2-109 Clock Video Output AXI Register Description

Offset	16'hec		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 7 • Default: 2 • Min: 2 • Typical: 2

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Clock NOC Display AXI

Table 2-110 Clock NOC Display AXI Register Description

Offset	16'hf0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Video Output AHB

Table 2-111 Clock Video Output AHB Register Description

Offset	16'hf4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Video Output AXI

Table 2-112 Clock Video Output AXI Register Description

Offset	16'hf8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock Video Output HDMI TX0 MCLK

Table 2-113 Clock Video Output HDMI TX0 MCLK Register Description

Offset	16'hfc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Video Output MIPI PHY Reference

Table 2-114 Clock Video Output MIPI PHY Reference Register Description

Offset	16'h100		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

Clock JPEG Codec AXI

Table 2-115 Clock JPEG Codec AXI Register Description

Offset	16'h104		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd6	Clock divider coefficient: • Max: 16 • Default: 6

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Table 2-115 Clock JPEG Codec AXI Register Description (continued)

Offset	16'h104		
Access	RW		
Bit	Name	Default	Description
			• Min: 6 • Typical: 6

CODAJ12 Clock AXI

Table 2-116 CODAJ12 Clock AXI Register Description

Offset	16'h108		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

CODAJ12 Clock Core

Table 2-117 CODAJ12 Clock Core Register Description

Offset	16'h10c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd6	Clock divider coefficient: • Max: 16 • Default: 6 • Min: 6 • Typical: 6

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CODAJ12 Clock APB

Table 2-118 CODAJ12 Clock APB Register Description

Offset	16'h110		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Video Decoder AXI

Table 2-119 Clock Video Decoder AXI Register Description

Offset	16'h114		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd3	Clock divider coefficient: • Max: 7 • Default: 3 • Min: 3 • Typical: 3

Clock WAVE511 AXI

Table 2-120 Clock WAVE511 AXI Register Description

Offset	16'h118		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock WAVE511 BPU

Table 2-121 Clock WAVE511 BPU Register Description

Offset	16'h11c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd3	Clock divider coefficient: • Max: 7 • Default: 3 • Min: 3 • Typical: 3

Clock WAVE511 VCE

Table 2-122 Clock WAVE511 VCE Register Description

Offset	16'h120		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 7 • Default: 2 • Min: 3 • Typical: 2

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Clock WAVE511 APB

Table 2-123 Clock WAVE511 APB Register Description

Offset	16'h124		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Video Decoder JPG ARB

Table 2-124 Clock Video Decoder JPG ARB Register Description

Offset	16'h128		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Video Decoder JPG Main

Table 2-125 Clock Video Decoder JPG Main Register Description

Offset	16'h12c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock NOC Video Decoder AXI

Table 2-126 Clock NOC Video Decoder AXI Register Description

Offset	16'h130		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Video Encoder AXI

Table 2-127 Clock Video Encoder AXI Register Description

Offset	16'h134		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd5	Clock divider coefficient: • Max: 15 • Default: 5 • Min: 5 • Typical: 5

Clock WAVE420L AXI

Table 2-128 Clock WAVE420L AXI Register Description

Offset	16'h138		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock WAVE420L BPU

Table 2-129 Clock WAVE420L BPU Register Description

Offset	16'h13c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd5	Clock divider coefficient: • Max: 15 • Default: 5 • Min: 5 • Typical: 5

Clock WAVE420L VCE

Table 2-130 Clock WAVE420L VCE Register Description

Offset	16'h140		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd5	Clock divider coefficient: • Max: 15 • Default: 5 • Min: 5 • Typical: 5

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Clock WAVE420L APB

Table 2-131 Clock WAVE420L APB Register Description

Offset	16'h144		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock NOC Video Encoder AXI

Table 2-132 Clock NOC Video Encoder AXI Register Description

Offset	16'h148		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock AXI Config 0 DEC Main Divider

Table 2-133 Clock AXI Config 0 DEC Main Divider Register Description

Offset	16'h14c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock AXI Config 0 DEC Main

Table 2-134 Clock AXI Config 0 DEC Main Register Description

Offset	16'h150		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock AXI Config 0 DEC HIFI4

Table 2-135 Clock AXI Config 0 DEC HIFI4 Register Description

Offset	16'h154		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock AXIMEM 128B AXI

Table 2-136 Clock AXIMEM 128B AXI Register Description

Offset	16'h158		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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QSPI Clock AHB

Table 2-137 QSPI Clock AHB Register Description

Offset	16'h15c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

QSPI Clock APB

Table 2-138 QSPI Clock APB Register Description

Offset	16'h160		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock QSPI Reference Source

Table 2-139 Clock QSPI Reference Source Register Description

Offset	16'h164		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd10	Clock divider coefficient: • Max: 16 • Default: 10 • Min: 10 • Typical: 10

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QSPI Clock Reference

Table 2-140 QSPI Clock Reference Register Description

Offset	16'h168		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_osc • clk_qspi_ref_src
[0:23]	Reserved	0	Reserved

U0 SD Clock AHB

Table 2-141 U0 SD Clock AHB Register Description

Offset	16'h16c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U1 SD Clock AHB

Table 2-142 U1 SD Clock AHB Register Description

Offset	16'h170		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U0 SD Card Clock

Table 2-143 U0 SD Card Clock Register Description

Offset	16'h174		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 15 • Default: 2 • Min: 2 • Typical: 2

U1 SD Card Clock

Table 2-144 U1 SD Card Clock Register Description

Offset	16'h178		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 15 • Default: 2 • Min: 2 • Typical: 2

Clock USB 125M

Table 2-145 Clock USB 125M Register Description

Offset	16'h17c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved

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Table 2-145 Clock USB 125M Register Description (continued)

Offset	16'h17c		
Access	RW		
Bit	Name	Default	Description
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd8	Clock divider coefficient: • Max: 15 • Default: 8 • Min: 12 • Typical: 10

Clock NOC STG AXI

Table 2-146 Clock NOC STG AXI Register Description

Offset	16'h180		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock GMAC 5 AXI 64 AHB

Table 2-147 Clock GMAC 5 AXI 64 AHB Register Description

Offset	16'h184		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock GMAC 5 AXI 64 AXI

Table 2-148 Clock GMAC 5 AXI 64 AXI Register Description

Offset	16'h188		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock GMAC Source

Table 2-149 Clock GMAC Source Register Description

Offset	16'h18c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 7 • Default: 2 • Min: 2 • Typical: 2

Clock GMAC 1 GTX

Table 2-150 Clock GMAC 1 GTX Register Description

Offset	16'h190		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd8	Clock divider coefficient: • Max: 15 • Default: 8

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Table 2-150 Clock GMAC 1 GTX Register Description (continued)

Offset	16'h190		
Access	RW		
Bit	Name	Default	Description
			• Min: 12 • Typical: 10

Clock GMAC 1 RMII RTX

Table 2-151 Clock GMAC 1 RMII RTX Register Description

Offset	16'h194		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 30 • Default: 2 • Min: 2 • Typical: 2

Clock GMAC 5 AXI 64 PTP

Table 2-152 Clock GMAC 5 AXI 64 PTP Register Description

Offset	16'h198		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd10	Clock divider coefficient: • Max: 31 • Default: 10 • Min: 15 • Typical: 10

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Clock GMAC 5 AXI 64 RX

Table 2-153 Clock GMAC 5 AXI 64 RX Register Description

Offset	16'h19c		
Access	RW		
Bit	Name	Default	Description
[31:24]	reserverd	0x0	Reserved
[23: 0]	dly_chain_sel	0x0	Selector delay chain stage number, totally 32 stages, -50 ps each stage. The register value indicates the delay chain stage number. For example, dly_chain_sel=1 means to delay 1 stage.

Clock GMAC 5 AXI 64 RX Inverter

Table 2-154 Clock GMAC 5 AXI 64 RX Inverter Register Description

Offset	16'h1a0		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock GMAC 5 AXI 64 TX

Table 2-155 Clock GMAC 5 AXI 64 TX Register Description

Offset	16'h1a4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_gmac1_gtxclk • clk_gmac1_rmii_rtx
[0:23]	Reserved	0	Reserved

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Clock GMAC 5 AXI 64 TX Inverter

Table 2-156 Clock GMAC 5 AXI 64 TX Inverter Register Description

Offset	16'h1a8		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock GMAC 1 GTXC

Table 2-157 Clock GMAC 1 GTXC Register Description

Offset	16'h1ac		
Access	RW		
Bit	Name	Default	Description
[31:24]	reserverd	0x0	Reserved
[23: 0]	dly_chain_sel	0x0	Selector delay chain stage number, totally 32 stages, -50 ps each stage. The register value indicates the delay chain stage number. For example, dly_chain_sel=1 means to delay 1 stage.

Clock GMAC 0 GTX

Table 2-158 Clock GMAC 0 GTX Register Description

Offset	16'h1b0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd8	Clock divider coefficient: • Max: 15 • Default: 8

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Table 2-158 Clock GMAC 0 GTX Register Description (continued)

Offset	16'h1b0		
Access	RW		
Bit	Name	Default	Description
			• Min: 12 • Typical: 10

Clock GMAC 0 PTP

Table 2-159 Clock GMAC 0 PTP Register Description

Offset	16'h1b4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd10	Clock divider coefficient: • Max: 31 • Default: 10 • Min: 15 • Typical: 25

Clock GMAC PHY

Table 2-160 Clock GMAC PHY Register Description

Offset	16'h1b8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd10	Clock divider coefficient: • Max: 31 • Default: 10 • Min: 15 • Typical: 25

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Clock GMAC 0 GTXC

Table 2-161 Clock GMAC 0 GTXC Register Description

Offset	16'h1bc		
Access	RW		
Bit	Name	Default	Description
[31:24]	reserverd	0x0	Reserved
[23: 0]	dly_chain_sel	0x0	Selector delay chain stage number, totally 32 stages, -50ps each stage. The register value indicates the delay chain stage number. For example, dly_chain_sel=1 means to delay 1 stage.

Clock SYS IOMUX PCLK

Table 2-162 Clock SYS IOMUX PCLK Register Description

Offset	16'h1c0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Mailbox APB

Table 2-163 Clock Mailbox APB Register Description

Offset	16'h1c4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock Internal Controller APB

Table 2-164 Clock Internal Controller APB Register Description

Offset	16'h1c8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U0 Clock CAN Controller APB

Table 2-165 U0 Clock CAN Controller APB Register Description

Offset	16'h1cc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U0 Clock CAN Controller Timer

Table 2-166 U0 Clock CAN Controller Timer Register Description

Offset	16'h1d0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd24	Clock divider coefficient: • Max: 24 • Default: 24

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Table 2-166 U0 Clock CAN Controller Timer Register Description (continued)

Offset	16'h1d0		
Access	RW		
Bit	Name	Default	Description
			• Min: 6 • Typical: 24

U0 Clock CAN Controller CAN

Table 2-167 U0 Clock CAN Controller CAN Register Description

Offset	16'h1d4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd8	Clock divider coefficient: • Max: 63 • Default: 8 • Min: 8 • Typical: 8

U1 Clock CAN Controller APB

Table 2-168 U1 Clock CAN Controller APB Register Description

Offset	16'h1d8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U1 Clock CAN Controller Timer

Table 2-169 U1 Clock CAN Controller Timer Register Description

Offset	16'h1dc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd24	Clock divider coefficient: • Max: 24 • Default: 24 • Min: 6 • Typical: 24

U1 Clock CAN Controller CAN

Table 2-170 U1 Clock CAN Controller CAN Register Description

Offset	16'h1e0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd8	Clock divider coefficient: • Max: 63 • Default: 8 • Min: 8 • Typical: 8

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Clock PWM APB

Table 2-171 Clock PWM APB Register Description

Offset	16'h1e4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock WDT APB

Table 2-172 Clock WDT APB Register Description

Offset	16'h1e8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock WDT

Table 2-173 Clock WDT Register Description

Offset	16'h1ec		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock Timer APB

Table 2-174 Clock Timer APB Register Description

Offset	16'h1f0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Timer 0

Table 2-175 Clock Timer 0 Register Description

Offset	16'h1f4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Timer 1

Table 2-176 Clock Timer 1 Register Description

Offset	16'h1f8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock Timer 2

Table 2-177 Clock Timer 2 Register Description

Offset	16'h1fc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Timer 3

Table 2-178 Clock Timer 3 Register Description

Offset	16'h200		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Temperature Sensor APB

Table 2-179 Clock Temperature Sensor APB Register Description

Offset	16'h204		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock Temperature Sensor

Table 2-180 Clock Temperature Sensor Register Description

Offset	16'h208		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd24	Clock divider coefficient: • Max: 24 • Default: 24 • Min: 24 • Typical: 24

U0 Clock SPI APB

Table 2-181 U0 Clock SPI APB Register Description

Offset	16'h20c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U1 Clock SPI APB

Table 2-182 U1 Clock SPI APB Register Description

Offset	16'h210		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved

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Table 2-182 U1 Clock SPI APB Register Description (continued)

Offset	16'h210		
Access	RW		
Bit	Name	Default	Description
[0:23]	Reserved	0	Reserved

U2 Clock SPI APB

Table 2-183 U2 Clock SPI APB Register Description

Offset	16'h214		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U3 Clock SPI APB

Table 2-184 U3 Clock SPI APB Register Description

Offset	16'h218		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U4 Clock SPI APB

Table 2-185 U4 Clock SPI APB Register Description

Offset	16'h21c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable

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Table 2-185 U4 Clock SPI APB Register Description (continued)

Offset	16'h21c		
Access	RW		
Bit	Name	Default	Description
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U5 Clock SPI APB

Table 2-186 U5 Clock SPI APB Register Description

Offset	16'h220		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U6 Clock SPI APB

Table 2-187 U6 Clock SPI APB Register Description

Offset	16'h224		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U0 Clock I2C APB

Table 2-188 U0 Clock I2C APB Register Description

Offset	16'h228		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U1 Clock I2C APB

Table 2-189 U1 Clock I2C APB Register Description

Offset	16'h22c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U2 Clock I2C APB

Table 2-190 U2 Clock I2C APB Register Description

Offset	16'h230		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U3 Clock I2C APB

Table 2-191 U3 Clock I2C APB Register Description

Offset	16'h234		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U4 Clock I2C APB

Table 2-192 U4 Clock I2C APB Register Description

Offset	16'h238		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U5 Clock I2C APB

Table 2-193 U5 Clock I2C APB Register Description

Offset	16'h23c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U6 Clock I2C APB

Table 2-194 U6 Clock I2C APB Register Description

Offset	16'h240		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U0 Clock UART APB

Table 2-195 U0 Clock UART APB Register Description

Offset	16'h244		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U0 Clock UART Core

Table 2-196 U0 Clock UART Core Register Description

Offset	16'h248		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U1 Clock UART APB

Table 2-197 U1 Clock UART APB Register Description

Offset	16'h24c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U1 Clock UART Core

Table 2-198 U1 Clock UART Core Register Description

Offset	16'h250		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U2 Clock UART APB

Table 2-199 U2 Clock UART APB Register Description

Offset	16'h254		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U2 Clock UART Core

Table 2-200 U2 Clock UART Core Register Description

Offset	16'h258		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U3 Clock UART APB

Table 2-201 U3 Clock UART APB Register Description

Offset	16'h25c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U3 Clock UART Core

Table 2-202 U3 Clock UART Core Register Description

Offset	16'h260		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2560	Clock divider coefficient: • Max: 131,071 • Default: 2,560

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Table 2-202 U3 Clock UART Core Register Description (continued)

Offset	16'h260		
Access	RW		
Bit	Name	Default	Description
			• Min: 2,560 • Typical: 2,560

U4 Clock UART APB

Table 2-203 U4 Clock UART APB Register Description

Offset	16'h264		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U4 Clock UART Core

Table 2-204 U4 Clock UART Core Register Description

Offset	16'h268		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2560	Clock divider coefficient: • Max: 131,071 • Default: 2,560 • Min: 2,560 • Typical: 2,560

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U5 Clock UART APB

Table 2-205 U5 Clock UART APB Register Description

Offset	16'h26c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U5 Clock UART Core

Table 2-206 U5 Clock UART Core Register Description

Offset	16'h270		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2560	Clock divider coefficient: • Max: 131,071 • Default: 2,560 • Min: 2,560 • Typical: 2,560

Clock PWMDAC APB

Table 2-207 Clock PWMDAC APB Register Description

Offset	16'h274		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved

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Table 2-207 Clock PWMDAC APB Register Description (continued)

Offset	16'h274		
Access	RW		
Bit	Name	Default	Description
[0:23]	Reserved	0	Reserved

Clock PWMDAC Core

Table 2-208 Clock PWMDAC Core Register Description

Offset	16'h278		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd12	Clock divider coefficient: • Max: 256 • Default: 12 • Min: 12 • Typical: 12

Clock SPDIF APB

Table 2-209 Clock SPDIF APB Register Description

Offset	16'h27c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock SPDIF Core

Table 2-210 Clock SPDIF Core Register Description

Offset	16'h280		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U0 Clock I2S TX APB

Table 2-211 U0 Clock I2S TX APB Register Description

Offset	16'h284		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock I2S TX 0 BCLK MST

Table 2-212 U0 Clock I2S TX 0 BCLK MST Register Description

Offset	16'h288		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd4	Clock divider coefficient: • Max: 32 • Default: 4

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Table 2-212 U0 Clock I2S TX 0 BCLK MST Register Description (continued)

Offset	16'h288		
Access	RW		
Bit	Name	Default	Description
			• Min: 4 • Typical: 4

Clock I2S TX 0 BCLK MST Inverter

Table 2-213 U0 Clock I2S TX 0 BCLK MST Inverter Register Description

Offset	16'h28c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock I2S TX 0 LRCK MST

Table 2-214 U0 Clock I2S TX 0 LRCK MST Register Description

Offset	16'h290		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_i2stx_4ch0_bclk_mst_inv • clk_i2stx_4ch0_bclk_mst
[0:23]	clk_divcfg	24'd64	Clock divider coefficient: • Max: 64 • Default: 64 • Min: 64 • Typical: 64

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U0 Clock I2S TX BCLK

Table 2-215 U0 Clock I2S TX BCLK Register Description

Offset	16'h294		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_i2stx_4ch0_bclk_mst • clk_i2stx_bclk_ext
[0:23]	Reserved	0	Reserved

U0 Clock I2S TX BCLK Negative

Table 2-216 U0 Clock I2S TX BCLK Negative Register Description

Offset	16'h298		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U0 Clock I2S TX LRCK

Table 2-217 U0 Clock I2S TX LRCK Register Description

Offset	16'h29c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_i2stx_4ch0_lrck_mst • clk_i2stx_lrck_ext
[0:23]	Reserved	0	Reserved

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U1 Clock I2S TX APB

Table 2-218 U1 Clock I2S TX APB Register Description

Offset	16'h2a0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock I2S TX 1 BCLK MST

Table 2-219 Clock I2S TX 1 BCLK MST Register Description

Offset	16'h2a4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd4	Clock divider coefficient: • Max: 32 • Default: 4 • Min: 4 • Typical: 4

Clock I2S TX 1 BCLK MST Inverter

Table 2-220 Clock I2S TX 1 BCLK MST Inverter Register Description

Offset	16'h2a8		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer
[24:29]	Reserved	0	Reserved

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Table 2-220 Clock I2S TX 1 BCLK MST Inverter Register Description (continued)

Offset	16'h2a8		
Access	RW		
Bit	Name	Default	Description
[0:23]	Reserved	0	Reserved

Clock I2S TX 1 BCLK MST

Table 2-221 Clock I2S TX 1 BCLK MST Register Description

Offset	16'h2ac		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_i2stx_4ch1_bclk_mst_inv • clk_i2stx_4ch1_bclk_mst
[0:23]	clk_divcfg	24'd64	Clock divider coefficient: • Max: 64 • Default: 64 • Min: 64 • Typical: 64

U1 Clock I2S TX BCLK

Table 2-222 U1 Clock I2S TX BCLK Register Description

Offset	16'h2b0		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_i2stx_4ch1_bclk_mst • clk_i2stx_bclk_ext
[0:23]	Reserved	0	Reserved

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U1 Clock I2S TX BCLK Negative

Table 2-223 U1 Clock I2S TX BCLK Negative Register Description

Offset	16'h2b4		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U1 Clock I2S TX LRCK

Table 2-224 U1 Clock I2S TX LRCK Register Description

Offset	16'h2b8		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_i2stx_4ch1_lrck_mst • clk_i2stx_lrck_ext
[0:23]	Reserved	0	Reserved

Clock I2S APB

Table 2-225 Clock I2S APB Register Description

Offset	16'h2bc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock I2S BCLK MST

Table 2-226 Clock I2S BCLK MST Register Description

Offset	16'h2c0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd4	Clock divider coefficient: • Max: 32 • Default: 4 • Min: 4 • Typical: 4

Clock I2S BCLK MST Inverter

Table 2-227 Clock I2S BCLK MST Inverter Register Description

Offset	16'h2c4		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock I2S LRCK MST

Table 2-228 Clock I2S LRCK MST Register Description

Offset	16'h2c8		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector:

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Table 2-228 Clock I2S LRCK MST Register Description (continued)

Offset	16'h2c8		
Access	RW		
Bit	Name	Default	Description
			• clk_i2srx_3ch_bclk_mst_inv • clk_i2srx_3ch_bclk_mst
[0:23]	clk_divcfg	24'd64	Clock divider coefficient: • Max: 64 • Default: 64 • Min: 64 • Typical: 64

Clock I2S BCLK

Table 2-229 Clock I2S BCLK Register Description

Offset	16'h2cc		
Access	RW		
Bit	Name	Default	Description
31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_i2srx_3ch_bclk_mst • clk_i2srx_bclk_ext
[0:23]	Reserved	0	Reserved

Clock I2S BCLK Negative

Table 2-230 Clock I2S BCLK Negative Register Description

Offset	16'h2d0		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock I2S LRCK

Table 2-231 Clock I2S LRCK Register Description

Offset	16'h2d4		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_i2srx_3ch_lrck_mst • clk_i2srx_lrck_ext
[0:23]	Reserved	0	Reserved

Clock PDM DMIC

Table 2-232 Clock PDM DMIC Register Description

Offset	16'h2d8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd8	Clock divider coefficient: • Max: 64 • Default: 8 • Min: 8 • Typical: 8

Clock PDM APB

Table 2-233 Clock PDM APB Register Description

Offset	16'h2dc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved

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Table 2-233 Clock PDM APB Register Description (continued)

Offset	16'h2dc		
Access	RW		
Bit	Name	Default	Description
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock TDM AHB

Table 2-234 Clock TDM AHB Register Description

Offset	16'h2e0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock TDM APB

Table 2-235 Clock TDM APB Register Description

Offset	16'h2e4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock TDM Internal

Table 2-236 Clock TDM Internal Register Description

Offset	16'h2e8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd1	Clock divider coefficient: • Max: 64 • Default: 1 • Min: 1 • Typical: 1

Clock TDM

Table 2-237 Clock TDM Register Description

Offset	16'h2ec		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_tdm_internal • clk_tdm_ext
[0:23]	Reserved	0	Reserved

Clock TDM Negative

Table 2-238 Clock TDM Negative Register Description

Offset	16'h2f0		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: Clock inverter • 0: Clock buffer

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Table 2-238 Clock TDM Negative Register Description (continued)

Offset	16'h2f0		
Access	RW		
Bit	Name	Default	Description
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock JTAG Certification TRNG

Table 2-239 Clock JTAG Certification TRNG Clock Register Description

Offset	16'h2f4		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd4	Clock divider coefficient: • Max: 4 • Default: 4 • Min: 4 • Typical: 4

Software RESET 0 Address Selector

Table 2-240 Software RESET 0 Address Selector Register Description

Offset	16'h2f8		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_jtag2apb_presetn	0	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u0_sys_syscon_presetn	0	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_sys_iomux_presetn	0	• 1: Assert reset • 0: De-assert reset
[3]	rst_u0_u7mc_sft7110_rst_bus	0	• 1: Assert reset • 0: De-assert reset

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Table 2-240 Software RESET 0 Address Selector Register Description (continued)

Offset	16'h2f8		
Access	RW		
Bit	Name	Default	Description
[4]	rst_u0_u7mc_sft7110_debug_reset	0	• 1: Assert reset • 0: De-assert reset
[5]	rst_u0_u7mc_sft7110_rst_core0	0	• 1: Assert reset • 0: De-assert reset
[6]	rst_u0_u7mc_sft7110_rst_core1	0	• 1: Assert reset • 0: De-assert reset
[7]	rst_u0_u7mc_sft7110_rst_core2	0	• 1: Assert reset • 0: De-assert reset
[8]	rst_u0_u7mc_sft7110_rst_core3	0	• 1: Assert reset • 0: De-assert reset
[9]	rst_u0_u7mc_sft7110_rst_core4	0	• 1: Assert reset • 0: De-assert reset
[10]	rst_u0_u7mc_sft7110_rst_core0_st	0	• 1: Assert reset • 0: De-assert reset
[11]	rst_u0_u7mc_sft7110_rst_core1_st	0	• 1: Assert reset • 0: De-assert reset
[12]	rst_u0_u7mc_sft7110_rst_core2_st	0	• 1: Assert reset • 0: De-assert reset
[13]	rst_u0_u7mc_sft7110_rst_core3_st	0	• 1: Assert reset • 0: De-assert reset
[14]	rst_u0_u7mc_sft7110_rst_core4_st	0	• 1: Assert reset • 0: De-assert reset
[15]	rst_u0_u7mc_sft7110_trace_rst0	0	• 1: Assert reset • 0: De-assert reset
[16]	rst_u0_u7mc_sft7110_trace_rst1	0	• 1: Assert reset • 0: De-assert reset

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Table 2-240 Software RESET 0 Address Selector Register Description (continued)

Offset	16'h2f8		
Access	RW		
Bit	Name	Default	Description
[17]	rst_u0_u7mc_sft7110_trace_rst2	0	• 1: Assert reset • 0: De-assert reset
[18]	rst_u0_u7mc_sft7110_trace_rst3	0	• 1: Assert reset • 0: De-assert reset
[19]	rst_u0_u7mc_sft7110_trace_rst4	0	• 1: Assert reset • 0: De-assert reset
[20]	rst_u0_u7mc_sft7110_trace_com_rst	0	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u0_img_gpu_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u0_img_gpu_rstn_doma	1	• 1: Assert reset • 0: De-assert reset
[23]	rstn_u0_sft7110_noc_bus_reset_apb_-bus_n	0	• 1: Assert reset • 0: De-assert reset
[24]	rstn_u0_sft7110_noc_bus_reset_axicfg0_-axi_n	0	• 1: Assert reset • 0: De-assert reset
[25]	rstn_u0_sft7110_noc_bus_reset_cpu_axi_-n	0	• 1: Assert reset • 0: De-assert reset
[26]	rstn_u0_sft7110_noc_bus_reset_disp_-axi_n	0	• 1: Assert reset • 0: De-assert reset
[27]	rstn_u0_sft7110_noc_bus_reset_gpu_-axi_n	0	• 1: Assert reset • 0: De-assert reset
[28]	rstn_u0_sft7110_noc_bus_reset_isp_axi_n	0	• 1: Assert reset • 0: De-assert reset
[29]	rstn_u0_sft7110_noc_bus_reset_ddrc_n	0	• 1: Assert reset • 0: De-assert reset

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Table 2-240 Software RESET 0 Address Selector Register Description (continued)

Offset	16'h2f8		
Access	RW		
Bit	Name	Default	Description
[30]	rstn_u0_sft7110_noc_bus_reset_stg_axi_n	0	• 1: Assert reset • 0: De-assert reset
[31]	rstn_u0_sft7110_noc_bus_reset_vdec_-axi_n	0	• 1: Assert reset • 0: De-assert reset

Software RESET 1 Address Selector

Table 2-241 Software RESET 1 Address Selector Register Description

Offset	16'h2fc		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_sft7110_noc_bus_reset_venc_-axi_n	0	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u0_axi_cfg1_dec_rstn_ahb	0	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_axi_cfg1_dec_rstn_main	0	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_axi_cfg0_dec_rstn_main	0	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_axi_cfg0_dec_rstn_main_div	0	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_axi_cfg0_dec_rstn_hifi4	0	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_ddr_sft7110_rstn_axi	0	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u0_ddr_sft7110_rstn_osc	0	• 1: Assert reset • 0: De-assert reset

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Table 2-241 Software RESET 1 Address Selector Register Description (continued)

Offset	16'h2fc		
Access	RW		
Bit	Name	Default	Description
[8]	rstn_u0_ddr_sft7110_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_dom_isp_top_rstn_dom_isp_-top_ip_top_reset_n	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_dom_isp_top_rstn_dom_isp_-top_rstn_isp_axi	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_dom_vout_top_rstn_dom_vout_-top_rstn_vout_src	1	• 1: Assert reset • 0: De-assert reset
[12]	rstn_u0_CODAJ12_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[13]	rstn_u0_CODAJ12_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[14]	rstn_u0_CODAJ12_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[15]	rstn_u0_WAVE511_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[16]	rstn_u0_WAVE511_rstn_bpu	1	• 1: Assert reset • 0: De-assert reset
[17]	rstn_u0_WAVE511_rstn_vce	1	• 1: Assert reset • 0: De-assert reset
[18]	rstn_u0_WAVE511_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[19]	rstn_u0_vdec_jpg_arb_jpgresetn	0	• 1: Assert reset • 0: De-assert reset
[20]	rstn_u0_vdec_jpg_arb_mainresetn	0	• 1: Assert reset • 0: De-assert reset

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Table 2-241 Software RESET 1 Address Selector Register Description (continued)

Offset	16'h2fc		
Access	RW		
Bit	Name	Default	Description
[21]	rstn_u0_aximem_128b_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u0_wave420l_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[23]	rstn_u0_wave420l_rstn_bpu	1	• 1: Assert reset • 0: De-assert reset
[24]	rstn_u0_wave420l_rstn_vce	1	• 1: Assert reset • 0: De-assert reset
[25]	rstn_u0_wave420l_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[26]	rstn_u1_aximem_128b_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[27]	rstn_u2_aximem_128b_rstn_axi	0	• 1: Assert reset • 0: De-assert reset
[28]	rstn_u0_intmem_rom_sram_rstn_rom	0	• 1: Assert reset • 0: De-assert reset
[29]	rstn_u0_cdns_qspi_rstn_ahb	0	• 1: Assert reset • 0: De-assert reset
[30]	rstn_u0_cdns_qspi_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[31]	rstn_u0_cdns_qspi_rstn_ref	0	• 1: Assert reset • 0: De-assert reset

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Software RESET 2 Address Selector

Table 2-242 Software RESET 2 Address Selector Register Description

Offset	16'h300		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_sdio_rstn_ahb	0	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u1_sdio_rstn_ahb	0	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u1_gmac5_axi64_aresetn_i	1	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u1_gmac5_axi64_hreset_n	1	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_mailbox_presetn	0	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_ssp_spi_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u1_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u2_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u3_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u4_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u5_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u6_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset

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Table 2-242 Software RESET 2 Address Selector Register Description (continued)

Offset	16'h300		
Access	RW		
Bit	Name	Default	Description
[12]	rstn_u0_i2c_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[13]	rstn_u1_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[14]	rstn_u2_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[15]	rstn_u3_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[16]	rstn_u4_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[17]	rstn_u5_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[18]	rstn_u6_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[19]	rstn_u0_uart_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[20]	rstn_u0_uart_rstn_core	0	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u1_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u1_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[23]	rstn_u2_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[24]	rstn_u2_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset

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Table 2-242 Software RESET 2 Address Selector Register Description (continued)

Offset	16'h300		
Access	RW		
Bit	Name	Default	Description
[25]	rstn_u3_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[26]	rstn_u3_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[27]	rstn_u4_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[28]	rstn_u4_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[29]	rstn_u5_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[30]	rstn_u5_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[31]	rstn_u0_cdns_spdif_rstn_apb	1	• 1: Assert reset • 0: De-assert reset

Software RESET 3 Address Selector

Table 2-243 Software RESET 3 Address Selector Register Description

Offset	16'h304		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_pwmdac_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u0_pdm_4mic_rstn_dmic	1	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_pdm_4mic_rstn_apb	1	• 1: Assert reset • 0: De-assert reset

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Table 2-243 Software RESET 3 Address Selector Register Description (continued)

Offset	16'h304		
Access	RW		
Bit	Name	Default	Description
[3]	rstn_u0_i2srx_3ch_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_i2srx_3ch_rstn_bclk	1	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_i2stx_4ch_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_i2stx_4ch_rstn_bclk	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u1_i2stx_4ch_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u1_i2stx_4ch_rstn_bclk	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_tdm16slot_rstn_ahb	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_tdm16slot_rstn_tdm	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_tdm16slot_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[12]	rstn_u0_pwm_8ch_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[13]	rstn_u0_dskit_wdt_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[14]	rstn_u0_dskit_wdt_rstn_wdt	1	• 1: Assert reset • 0: De-assert reset
[15]	rstn_u0_can_ctrl_rstn_apb	1	• 1: Assert reset • 0: De-assert reset

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Table 2-243 Software RESET 3 Address Selector Register Description (continued)

Offset	16'h304		
Access	RW		
Bit	Name	Default	Description
[16]	rstn_u0_can_ctrl_rstn_can	1	• 1: Assert reset • 0: De-assert reset
[17]	rstn_u0_can_ctrl_rstn_timer	1	• 1: Assert reset • 0: De-assert reset
[18]	rstn_u1_can_ctrl_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[19]	rstn_u1_can_ctrl_rstn_can	1	• 1: Assert reset • 0: De-assert reset
[20]	rstn_u1_can_ctrl_rstn_timer	1	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u0_si5_timer_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u0_si5_timer_rstn_timer0	1	• 1: Assert reset • 0: De-assert reset
[23]	rstn_u0_si5_timer_rstn_timer1	1	• 1: Assert reset • 0: De-assert reset
[24]	rstn_u0_si5_timer_rstn_timer2	1	• 1: Assert reset • 0: De-assert reset
[25]	rstn_u0_si5_timer_rstn_timer3	1	• 1: Assert reset • 0: De-assert reset
[26]	rstn_u0_int_ctrl_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[27]	rstn_u0_temp_sensor_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[28]	rstn_u0_temp_sensor_rstn_temp	1	• 1: Assert reset • 0: De-assert reset

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Table 2-243 Software RESET 3 Address Selector Register Description (continued)

Offset	16'h304		
Access	RW		
Bit	Name	Default	Description
[29]	rstn_u0_jtag_certification_rst_n	0	• 1: Assert reset • 0: De-assert reset
[30:31]	Reserved	0	Reserved

SYSCRG RESET Status 0

Table 2-244 SYSCRG RESET Status 0 Register Description

Offset	16'h308		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_jtag2apb_presetn	1	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u0_sys_syscon_presetn	0	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_sys_iomux_presetn	0	• 1: Assert reset • 0: De-assert reset
[3]	rst_u0_u7mc_sft7110_rst_bus	0	• 1: Assert reset • 0: De-assert reset
[4]	rst_u0_u7mc_sft7110_debug_reset	0	• 1: Assert reset • 0: De-assert reset
[5]	rst_u0_u7mc_sft7110_rst_core0	0	• 1: Assert reset • 0: De-assert reset
[6]	rst_u0_u7mc_sft7110_rst_core1	0	• 1: Assert reset • 0: De-assert reset
[7]	rst_u0_u7mc_sft7110_rst_core2	0	• 1: Assert reset • 0: De-assert reset
[8]	rst_u0_u7mc_sft7110_rst_core3	0	• 1: Assert reset • 0: De-assert reset

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Table 2-244 SYSCRG RESET Status 0 Register Description (continued)

Offset	16'h308		
Access	RW		
Bit	Name	Default	Description
[9]	rst_u0_u7mc_sft7110_rst_core4	0	• 1: Assert reset • 0: De-assert reset
[10]	rst_u0_u7mc_sft7110_rst_core0_st	0	• 1: Assert reset • 0: De-assert reset
[11]	rst_u0_u7mc_sft7110_rst_core1_st	0	• 1: Assert reset • 0: De-assert reset
[12]	rst_u0_u7mc_sft7110_rst_core2_st	0	• 1: Assert reset • 0: De-assert reset
[13]	rst_u0_u7mc_sft7110_rst_core3_st	0	• 1: Assert reset • 0: De-assert reset
[14]	rst_u0_u7mc_sft7110_rst_core4_st	0	• 1: Assert reset • 0: De-assert reset
[15]	rst_u0_u7mc_sft7110_trace_rst0	0	• 1: Assert reset • 0: De-assert reset
[16]	rst_u0_u7mc_sft7110_trace_rst1	0	• 1: Assert reset • 0: De-assert reset
[17]	rst_u0_u7mc_sft7110_trace_rst2	0	• 1: Assert reset • 0: De-assert reset
[18]	rst_u0_u7mc_sft7110_trace_rst3	0	• 1: Assert reset • 0: De-assert reset
[19]	rst_u0_u7mc_sft7110_trace_rst4	0	• 1: Assert reset • 0: De-assert reset
[20]	rst_u0_u7mc_sft7110_trace_com_rst	0	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u0_img_gpu_rstn_apb	1	• 1: Assert reset • 0: De-assert reset

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Table 2-244 SYSCRG RESET Status 0 Register Description (continued)

Offset	16'h308		
Access	RW		
Bit	Name	Default	Description
[22]	rstn_u0_img_gpu_rstn_doma	1	• 1: Assert reset • 0: De-assert reset
[23]	rstn_u0_sft7110_noc_bus_reset_apb_bus_n	0	• 1: Assert reset • 0: De-assert reset
[24]	rstn_u0_sft7110_noc_bus_reset_axicfg0_axi_n	0	• 1: Assert reset • 0: De-assert reset
[25]	rstn_u0_sft7110_noc_bus_reset_cpu_axi_n	0	• 1: Assert reset • 0: De-assert reset
[26]	rstn_u0_sft7110_noc_bus_reset_disp_axi_n	0	• 1: Assert reset • 0: De-assert reset
[27]	rstn_u0_sft7110_noc_bus_reset_gpu_axi_n	0	• 1: Assert reset • 0: De-assert reset
[28]	rstn_u0_sft7110_noc_bus_reset_isp_axi_n	0	• 1: Assert reset • 0: De-assert reset
[29]	rstn_u0_sft7110_noc_bus_reset_ddrc_n	0	• 1: Assert reset • 0: De-assert reset
[30]	rstn_u0_sft7110_noc_bus_reset_stg_axi_n	0	• 1: Assert reset • 0: De-assert reset
[31]	rstn_u0_sft7110_noc_bus_reset_vdec_axi_n	0	• 1: Assert reset • 0: De-assert reset

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SYSCRG RESET Status 1

Table 2-245 SYSCRG RESET Status 1 Register Description

Offset	16'h30c		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_sft7110_noc_bus_reset_venc_-axi_n	0	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u0_axi_cfg1_dec_rstn_ahb	0	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_axi_cfg1_dec_rstn_main	0	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_axi_cfg0_dec_rstn_main	0	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_axi_cfg0_dec_rstn_main_div	0	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_axi_cfg0_dec_rstn_hifi4	0	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_ddr_sft7110_rstn_axi	0	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u0_ddr_sft7110_rstn_osc	0	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u0_ddr_sft7110_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_dom_isp_top_rstn_dom_isp_-top_ip_top_reset_n	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_dom_isp_top_rstn_dom_isp_-top_rstn_isp_axi	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_dom_vout_top_rstn_dom_vout_-top_rstn_vout_src	1	• 1: Assert reset • 0: De-assert reset

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Table 2-245 SYSCRG RESET Status 1 Register Description (continued)

Offset	16'h30c		
Access	RW		
Bit	Name	Default	Description
[12]	rstn_u0_CODAJ12_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[13]	rstn_u0_CODAJ12_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[14]	rstn_u0_CODAJ12_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[15]	rstn_u0_WAVE511_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[16]	rstn_u0_WAVE511_rstn_bpu	1	• 1: Assert reset • 0: De-assert reset
[17]	rstn_u0_WAVE511_rstn_vce	1	• 1: Assert reset • 0: De-assert reset
[18]	rstn_u0_WAVE511_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[19]	rstn_u0_vdec_jpg_arb_jpgresetn	0	• 1: Assert reset • 0: De-assert reset
[20]	rstn_u0_vdec_jpg_arb_mainresetn	0	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u0_aximem_128b_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u0_wave420l_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[23]	rstn_u0_wave420l_rstn_bpu	1	• 1: Assert reset • 0: De-assert reset
[24]	rstn_u0_wave420l_rstn_vce	1	• 1: Assert reset • 0: De-assert reset

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Table 2-245 SYSCRG RESET Status 1 Register Description (continued)

Offset	16'h30c		
Access	RW		
Bit	Name	Default	Description
[25]	rstn_u0_wave420l_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[26]	rstn_u1_aximem_128b_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[27]	rstn_u2_aximem_128b_rstn_axi	0	• 1: Assert reset • 0: De-assert reset
[28]	rstn_u0_intmem_rom_sram_rstn_rom	0	• 1: Assert reset • 0: De-assert reset
[29]	rstn_u0_cdns_qspi_rstn_ahb	0	• 1: Assert reset • 0: De-assert reset
[30]	rstn_u0_cdns_qspi_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[31]	rstn_u0_cdns_qspi_rstn_ref	0	• 1: Assert reset • 0: De-assert reset

SYSCRG RESET Status 2

Table 2-246 SYSCRG RESET Status 2 Register Description

Offset	16'h310		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_sdio_rstn_ahb	0	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u1_sdio_rstn_ahb	0	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u1_gmac5_axi64_aresetn_i	1	• 1: Assert reset • 0: De-assert reset

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Table 2-246 SYSCRG RESET Status 2 Register Description (continued)

Offset	16'h310		
Access	RW		
Bit	Name	Default	Description
[3]	rstn_u1_gmac5_axi64_hreset_n	1	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_mailbox_presetn	0	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_ssp_spi_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u1_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u2_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u3_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u4_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u5_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u6_ssp_spi_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[12]	rstn_u0_i2c_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[13]	rstn_u1_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[14]	rstn_u2_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[15]	rstn_u3_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset

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Table 2-246 SYSCRG RESET Status 2 Register Description (continued)

Offset	16'h310		
Access	RW		
Bit	Name	Default	Description
[16]	rstn_u4_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[17]	rstn_u5_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[18]	rstn_u6_i2c_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[19]	rstn_u0_uart_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[20]	rstn_u0_uart_rstn_core	0	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u1_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u1_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[23]	rstn_u2_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[24]	rstn_u2_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[25]	rstn_u3_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[26]	rstn_u3_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[27]	rstn_u4_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[28]	rstn_u4_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset

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Table 2-246 SYSCRG RESET Status 2 Register Description (continued)

Offset	16'h310		
Access	RW		
Bit	Name	Default	Description
[29]	rstn_u5_uart_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[30]	rstn_u5_uart_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[31]	rstn_u0_cdns_spdif_rstn_apb	1	• 1: Assert reset • 0: De-assert reset

SYSCRG RESET Status 3

Table 2-247 SYSCRG RESET Status 3 Register Description

Offset	16'h314		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_pwmdac_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u0_pdm_4mic_rstn_dmic	1	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_pdm_4mic_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_i2srx_3ch_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_i2srx_3ch_rstn_bclk	1	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_i2stx_4ch_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_i2stx_4ch_rstn_bclk	1	• 1: Assert reset • 0: De-assert reset

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Table 2-247 SYSCRG RESET Status 3 Register Description (continued)

Offset	16'h314		
Access	RW		
Bit	Name	Default	Description
[7]	rstn_u1_i2stx_4ch_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u1_i2stx_4ch_rstn_bclk	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_tdm16slot_rstn_ahb	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_tdm16slot_rstn_tdm	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_tdm16slot_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[12]	rstn_u0_pwm_8ch_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[13]	rstn_u0_dskit_wdt_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[14]	rstn_u0_dskit_wdt_rstn_wdt	1	• 1: Assert reset • 0: De-assert reset
[15]	rstn_u0_can_ctrl_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[16]	rstn_u0_can_ctrl_rstn_can	1	• 1: Assert reset • 0: De-assert reset
[17]	rstn_u0_can_ctrl_rstn_timer	1	• 1: Assert reset • 0: De-assert reset
[18]	rstn_u1_can_ctrl_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[19]	rstn_u1_can_ctrl_rstn_can	1	• 1: Assert reset • 0: De-assert reset

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Table 2-247 SYSCRG RESET Status 3 Register Description (continued)

Offset	16'h314		
Access	RW		
Bit	Name	Default	Description
[20]	rstn_u1_can_ctrl_rstn_timer	1	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u0_si5_timer_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u0_si5_timer_rstn_timer0	1	• 1: Assert reset • 0: De-assert reset
[23]	rstn_u0_si5_timer_rstn_timer1	1	• 1: Assert reset • 0: De-assert reset
[24]	rstn_u0_si5_timer_rstn_timer2	1	• 1: Assert reset • 0: De-assert reset
[25]	rstn_u0_si5_timer_rstn_timer3	1	• 1: Assert reset • 0: De-assert reset
[26]	rstn_u0_int_ctrl_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[27]	rstn_u0_temp_sensor_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[28]	rstn_u0_temp_sensor_rstn_temp	1	• 1: Assert reset • 0: De-assert reset
[29]	rstn_u0_jtag_certification_rst_n	0	• 1: Assert reset • 0: De-assert reset
[30:31]	reserved	0	reserved

2.8.2. STG CRG

The JH-7110 system provides the following STG CRG control registers.

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Clock HIFI4 Core

Table 2-248 Clock HIFI4 Core Register Description

Offset	16'h0		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock USB APB

Table 2-249 Clock USB APB Register Description

Offset	16'h4		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock USB UTMI APB

Table 2-250 Clock USB UTMI APB Register Description

Offset	16'h8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock USB AXI

Table 2-251 Clock USB AXI Register Description

Offset	16'hc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved

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Table 2-251 Clock USB AXI Register Description (continued)

Offset	16'hc		
Access	RW		
Bit	Name	Default	Description
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock USB IPM

Table 2-252 Clock USB IPM Register Description

Offset	16'h10		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

Clock USB STB

Table 2-253 Clock USB STB Register Description

Offset	16'h14		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd4	Clock divider coefficient: • Max: 4 • Default: 4 • Min: 4 • Typical: 4

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Clock USB APP 125

Table 2-254 Clock USB APP 125 Register Description

Offset	16'h18		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock USB Reference Clock

Table 2-255 Clock USB Reference Clock Register Description

Offset	16'h1c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 2 • Default: 2 • Min: 2 • Typical: 2

U0 Clock PCIe AXI MST 0

Table 2-256 U0 Clock PCIe AXI MST 0 Register Description

Offset	16'h20		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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U0 Clock PCIe APB

Table 2-257 U0 Clock PCIe APB Register Description

Offset	16'h24		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U0 Clock PCIe TL

Table 2-258 U0 Clock PCIe TL Register Description

Offset	16'h28		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U1 Clock PCIe AXI MST 0

Table 2-259 U1 Clock PCIe AXI MST 0 Register Description

Offset	16'h2c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U1 Clock PCIe APB

Table 2-260 U1 Clock PCIe APB Register Description

Offset	16'h30		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved

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Table 2-260 U1 Clock PCIe APB Register Description (continued)

Offset	16'h30		
Access	RW		
Bit	Name	Default	Description
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

U1 Clock PCIe TL

Table 2-261 U1 Clock PCIe TL Register Description

Offset	16'h34		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock PCIe 01 SLV DEC Main

Table 2-262 Clock PCIe 01 SLV DEC Main Register Description

Offset	16'h38		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock Security HCLK

Table 2-263 Clock Security HCLK Register Description

Offset	16'h3c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock Security Miscellaneous AHB

Table 2-264 Clock Security Miscellaneous AHB Register Description

Offset	16'h40		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock STG MTRX Group 0 Main

Table 2-265 Clock STG MTRX Group 0 Main Register Description

Offset	16'h44		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock STG MTRX Group 0 Bus

Table 2-266 Clock STG MTRX Group 0 Bus Register Description

Offset	16'h48		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock STG MTRX Group 0 STG

Table 2-267 Clock STG MTRX Group 0 STG Register Description

Offset	16'h4c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved

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Table 2-267 Clock STG MTRX Group 0 STG Register Description (continued)

Offset	16'h4c		
Access	RW		
Bit	Name	Default	Description
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock STG MTRX Group 1 Main

Table 2-268 Clock STG MTRX Group 1 Main Register Description

Offset	16'h50		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock STG MTRX Group 1 Bus

Table 2-269 Clock STG MTRX Group 1 Bus Register Description

Offset	16'h54		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock STG MTRX Group 1 STG

Table 2-270 Clock STG MTRX Group 1 STG Register Description

Offset	16'h58		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock STG MTRX Group 1 HIFI

Table 2-271 Clock STG MTRX Group 1 HIFI Register Description

Offset	16'h5c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock E2 RTC

Table 2-272 Clock E2 RTC Register Description

Offset	16'h60		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd24	Clock divider coefficient: • Max: 24 • Default: 24 • Min: 24 • Typical: 24

Clock E2 Core

Table 2-273 Clock E2 Core Register Description

Offset	16'h64		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Clock E2 DBG

Table 2-274 Clock E2 DBG Register Description

Offset	16'h68		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock DMA AXI

Table 2-275 Clock DMA AXI Register Description

Offset	16'h6c		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Clock DMA AHB

Table 2-276 Clock DMA AHB Register Description

Offset	16'h70		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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Software RESET Address Selector

Table 2-277 Software RESET Address Selector Register Description

Offset	16'h74		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_stg_syscon_presetn	0	• 1: Assert reset • 0: De-assert reset
[1]	rst_u0_hifi4_rst_core	1	• 1: Assert reset • 0: De-assert reset
[2]	rst_u0_hifi4_rst_axi	1	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_sec_top_hresetn	1	• 1: Assert reset • 0: De-assert reset
[4]	rst_u0_e2_sft7110_rst_core	1	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_dma1p_8ch_56hs_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_dma1p_8ch_56hs_rstn_ahb	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u0_cdn_usb_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u0_cdn_usb_rstn_usb_apb	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_cdn_usb_rstn_utmi_apb	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_cdn_usb_rstn_pwrup	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_plda_pcie_rstn_axi_mst0	1	• 1: Assert reset • 0: De-assert reset

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Table 2-277 Software RESET Address Selector Register Description (continued)

Offset	16'h74		
Access	RW		
Bit	**Name**	**Default**	**Description**
[12]	rstn_u0_plda_pcie_rstn_axi_slv0	1	• 1: Assert reset • 0: De-assert reset
[13]	rstn_u0_plda_pcie_rstn_axi_slv	1	• 1: Assert reset • 0: De-assert reset
[14]	rstn_u0_plda_pcie_rstn_brg	1	• 1: Assert reset • 0: De-assert reset
[15]	rstn_u0_plda_pcie_rstn_pcie	1	• 1: Assert reset • 0: De-assert reset
[16]	rstn_u0_plda_pcie_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[17]	rstn_u1_plda_pcie_rstn_axi_mst0	1	• 1: Assert reset • 0: De-assert reset
[18]	rstn_u1_plda_pcie_rstn_axi_slv0	1	• 1: Assert reset • 0: De-assert reset
[19]	rstn_u1_plda_pcie_rstn_axi_slv	1	• 1: Assert reset • 0: De-assert reset
[20]	rstn_u1_plda_pcie_rstn_brg	1	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u1_plda_pcie_rstn_pcie	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u1_plda_pcie_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[31:23]	Reserved	0	Reserved

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STGCRG RESET Status

Table 2-278 STGCRG RESET Status Register Description

Offset	16'h78		
Access	RW		
Bit	Name	Default	Description
[0]	rstn_u0_stg_syscon_presetn	0	• 1: Assert reset • 0: De-assert reset
[1]	rst_u0_hifi4_rst_core	1	• 1: Assert reset • 0: De-assert reset
[2]	rst_u0_hifi4_rst_axi	1	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_sec_top_hresetn	1	• 1: Assert reset • 0: De-assert reset
[4]	rst_u0_e2_sft7110_rst_core	1	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_dma1p_8ch_56hs_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_dma1p_8ch_56hs_rstn_ahb	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u0_cdn_usb_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u0_cdn_usb_rstn_usb_apb	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_cdn_usb_rstn_utmi_apb	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_cdn_usb_rstn_pwrup	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_plda_pcie_rstn_axi_mst0	1	• 1: Assert reset • 0: De-assert reset

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Table 2-278 STGCRG RESET Status Register Description (continued)

Offset	16'h78		
Access	RW		
Bit	Name	Default	Description
[12]	rstn_u0_plda_pcie_rstn_axi_slv0	1	• 1: Assert reset • 0: De-assert reset
[13]	rstn_u0_plda_pcie_rstn_axi_slv	1	• 1: Assert reset • 0: De-assert reset
[14]	rstn_u0_plda_pcie_rstn_brg	1	• 1: Assert reset • 0: De-assert reset
[15]	rstn_u0_plda_pcie_rstn_pcie	1	• 1: Assert reset • 0: De-assert reset
[16]	rstn_u0_plda_pcie_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[17]	rstn_u1_plda_pcie_rstn_axi_mst0	1	• 1: Assert reset • 0: De-assert reset
[18]	rstn_u1_plda_pcie_rstn_axi_slv0	1	• 1: Assert reset • 0: De-assert reset
[19]	rstn_u1_plda_pcie_rstn_axi_slv	1	• 1: Assert reset • 0: De-assert reset
[20]	rstn_u1_plda_pcie_rstn_brg	1	• 1: Assert reset • 0: De-assert reset
[21]	rstn_u1_plda_pcie_rstn_pcie	1	• 1: Assert reset • 0: De-assert reset
[22]	rstn_u1_plda_pcie_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[31:23]	Reserved	0	Reserved

2.8.3. AON CRG

The JH-7110 system provides the following AON CRG Always-ON (AON) control registers.

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Oscillator Clock

Table 2-279 Oscillator Clock Register Description

Offset	16'h0		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd4	Clock divider coefficient: • Max: 4 • Default: 4 • Min: 4 • Typical: 4

AON APB Function Clock

Table 2-280 AON APB Function Clock Register Description

Offset	16'h4		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_osc_div4 • clk_osc
[0:23]	Reserved	0	Reserved

AHB GMAC5 Clock

Table 2-281 AHB GMAC5 Clock Register Description

Offset	16'h8		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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AXI GMAC5 Clock

Table 2-282 AXI GMAC5 Clock Register Description

Offset	16'hc		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

GMAC0 RMII RTX Clock

Table 2-283 GMAC0 RMII RTX Clock Register Description

Offset	16'h10		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd2	Clock divider coefficient: • Max: 30 • Default: 2 • Min: 2 • Typical: 2

GMAC5 AXI64 Clock Transmitter

Table 2-284 GMAC5 AXI64 Clock Transmitter Register Description

Offset	16'h14		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • u0_sys_crg.clk_gmac0_gtxclk • clk_gmac0_rmii_rtx
[0:23]	Reserved	0	Reserved

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GMAC5 AXI64 Clock Transmission Inverter

Table 2-285 GMAC5 AXI64 Clock Transmission Inverter Register Description

Offset	16'h18		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	1: Clock inverter / 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

GMAC5 AXI64 Clock Receiver

Table 2-286 GMAC5 AXI64 Clock Receiver Register Description

Offset	16'h1c		
Access	RW		
Bit	Name	Default	Description
[31:24]	reserverd	0x0	Reserved
[23: 0]	dly_chain_sel	0x0	Selector delay chain stage number, totally 32 stages, -50ps each stage. The register value indicates the delay chain stage number. For example, dly_chain_sel=1 means to delay 1 stage.

GMAC5 AXI64 Clock Receiving Inverter

Table 2-287 GMAC5 AXI64 Clock Receiving Inverter Register Description

Offset	16'h20		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	1: Clock inverter / 0: Clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

OPTC APB Clock

Table 2-288 OPTC APB Clock Register Description

Offset	16'h24		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable

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Table 2-288 OPTC APB Clock Register Description (continued)

Offset	16'h24		
Access	RW		
Bit	Name	Default	Description
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

RTC HMS APB Clock

Table 2-289 RTC HMS APB Clock Register Description

Offset	16'h28		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	1	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

RTC Internal Clock

Table 2-290 RTC Internal Clock Register Description

Offset	16'h2c		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'd750	Clock divider coefficient: • Max: 1,022 • Default: 750 • Min: 750 • Typical: 750

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RTC HMS Clock Oscillator 32K

Table 2-291 RTC HMS Clock Oscillator 32K Register Description

Offset	16'h30		
Access	RW		
Bit	Name	Default	Description
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6'd0	Clock multiplexing selector: • clk_rtc • clk_rtc_internal
[0:23]	Reserved	0	Reserved

RTC HMS Clock Calculator

Table 2-292 RTC HMS Clock Calculator Register Description

Offset	16'h34		
Access	RW		
Bit	Name	Default	Description
[31]	clk_icg	0	1: Clock enable / 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Software RESET Address Selector

Table 2-293 Software RESET Address Selector Register Description

Offset	16'h38		
Access	RW		
Bit	Name	Default	Description
[0]	gmac5_axi64_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[1]	gmac5_axi64_rstn_ahb	1	• 1: Assert reset • 0: De-assert reset
[2]	aon_iomux_presetn	0	• 1: Assert reset • 0: De-assert reset
[3]	pmu_rstn_apb	0	• 1: Assert reset • 0: De-assert reset

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Table 2-293 Software RESET Address Selector Register Description (continued)

Offset	16'h38		
Access	RW		
Bit	Name	Default	Description
[4]	pmu_rstn_wkup	0	• 1: Assert reset • 0: De-assert reset
[5]	rtc_hms_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[6]	rtc_hms_rstn_cal	1	• 1: Assert reset • 0: De-assert reset
[7]	rtc_hms_rstn_osc32k	1	• 1: Assert reset • 0: De-assert reset
[8:31]	Reserved	0	Reserved

AONCRG Reset Status

Table 2-294 AONCRG Reset Status Register Description

Offset	16'h3c		
Access	RW		
Bit	Name	Default	Description
[0]	gmac5_axi64_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[1]	gmac5_axi64_rstn_ahb	1	• 1: Assert reset • 0: De-assert reset
[2]	aon_iomux_presetn	0	• 1: Assert reset • 0: De-assert reset
[3]	pmu_rstn_apb	0	• 1: Assert reset • 0: De-assert reset
[4]	pmu_rstn_wkup	0	• 1: Assert reset • 0: De-assert reset
[5]	rtc_hms_rstn_apb	1	• 1: Assert reset • 0: De-assert reset

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Table 2-294 AONCRG Reset Status Register Description (continued)

Offset	16'h3c		
Access	RW		
Bit	Name	Default	Description
[6]	rtc_hms_rstn_cal	1	• 1: Assert reset • 0: De-assert reset
[7]	rtc_hms_rstn_osc32k	1	• 1: Assert reset • 0: De-assert reset
[8:31]	Reserved	0	Reserved

2.8.4. SYS SYSCON

The JH-7110 system provides the following SYS SYSCON system control registers which provides clock and reset signals to interfaces with master and/or slave signals.

SYS SYSCONSAIF SYSCFG 0

Table 2-295 SYS SYSCONSAIF SYSCFG 0 Register Description

Offset	0x0			
Default	0x0			
Bit	Name	Access	Default	Description
[3:0]	SCFG_e24_remap_haddr	WR	0x0	
[4:7]	SCFG_hifi4_idma_remap_araddr	WR	0x0	
[11:8]	SCFG_hifi4_idma_remap_awaddr	WR	0x0	
[15:12]	SCFG_hifi4_sys_remap_araddr	WR	0x0	
[19:16]	SCFG_hifi4_sys_remap_awaddr	WR	0x0	
[23:20]	SCFG_jpg_remap_araddr	WR	0x0	
[27:24]	SCFG_jpg_remap_awaddr	WR	0x0	
[31:28]	SCFG_sd0_remap_araddr	WR	0x0	

SYS SYSCONSAIF SYSCFG 4

Table 2-296 SYS SYSCONSAIF SYSCFG 4 Register Description

Offset	0x4			
Default	0x0			
Bit	Name	Access	Default	Description
[3:0]	SCFG_sd1_remap_awaddr	WR	0x0	
[4:7]	SCFG_sec_haddr_remap	WR	0x0	
[11:8]	SCFG_usb_araddr_remap	WR	0x0	

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Table 2-296 SYS SYSCONSAIF SYSCFG 4 Register Description (continued)

Offset	0x4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[15:12]	SCFG_usb_awaddr_remap	WR	0x0	
[19:16]	SCFG_vdec_remap_awaddr	WR	0x0	
[23:20]	SCFG_venc_remap_araddr	WR	0x0	
[27:24]	SCFG_venc_remap_awaddr	WR	0x0	
[31:28]	SCFG_vout0_remap_araddr	WR	0x0	

SYS SYSCONSAIF SYSCFG 8

Table 2-297 SYS SYSCONSAIF SYSCFG 8 Register Description

Offset	0x8			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[3:0]	SCFG_vout0_remap_awaddr	WR	0x0	
[4:7]	SCFG_vout1_remap_araddr	WR	0x0	
[11:8]	SCFG_vout1_remap_awaddr	WR	0x0	
[31:12]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 12

Table 2-298 SYS SYSCONSAIF SYSCFG 12 Register Description

Offset	16'h0			
Access	**RW**			
Bit	**Name**	**Access**	**Default**	**Description**
[31]	Reserved		0	Reserved
[3:0]	SYSCFG_gpio_sel18_cfg	WR	0x0	Set the GPIO voltage of all the 4 GPIO groups in this field: • Bit 0 = 0 : GPIO Group 0 (GPIO21-35) voltage select 3.3 V • Bit 0 = 1 : GPIO Group 0 (GPIO21-35) voltage select 1.8 V • Bit 1 = 0 : GPIO Group 1 (GPIO36-63) voltage select 3.3 V • Bit 1 = 1 : GPIO Group 1 (GPIO36-63) voltage select 1.38V • Bit 2 = 0 : GPIO Group 2 (GPIO0-6) voltage select 3.3 V

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Table 2-298 SYS SYSCONSAIF SYSCFG 12 Register Description (continued)

Offset	16'h0			
Access	RW			
Bit	Name	Access	Default	Description
				• Bit 2 = 1: GPIO Group 2 (GPIO0-6) voltage select 1.8 V • Bit 3 = 0 : GPIO Group 3 (GPIO7-20) voltage select 3.3 V • Bit 3 = 1 : GPIO Group 3 (GPIO7-20) voltage select 1.8 V
[31:4]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 16

Table 2-299 SYS SYSCONSAIF SYSCFG 16 Register Description

Offset	0x10			
Default	0x0			
Bit	Name	Access	Default	Description
[1:0]	u0_CODAJ12_o_cur_inst_a	RO	0x0	Tie 0 in jpu internal, do not care
[2]	u0_WAVE511_o_vpu_idle	RO	0x0	VPU monitoring signal
[3]	u0_can_ctrl_can_fd_enable	WR	0x0	
[4]	u0_can_ctrl_host_ecc_disable	WR	0x0	
[23:5]	u0_can_ctrl_host_if	RO	0x0	
[28:24]	u0_cdns_qspi_SCFG_qspi_sclk_dlychain_sel	WR	0x0	des_qspi_sclk_dla:clock delay
[31:29]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 20

Table 2-300 SYS SYSCONSAIF SYSCFG 20 Register Description

Offset	0x14			
Default	0xd54d54			
Bit	Name	Access	Default	Description
[0:11]	u0_cdns_qspi_SCFG_sram_config	WR	0xd54	SRAM/ROM configuration. • [0]: SLP, sleep enable, high active, default is low. • [1]: SD, shutdown enable, high active, default is low. • [2:3]: RTSEL, timing setting for debug purpose, default is 2'b01

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Table 2-300 SYS SYSCONSAIF SYSCFG 20 Register Description (continued)

Offset	0x14			
Default	**0xd54d54**			
Bit	**Name**	**Access**	**Default**	**Description**
				• [4:5]: PTSEL, timing setting for debug purpose, default is 2'b01 • [6:7]: TRB, timing setting for debug purpose, default is 2'b01 • [8:9]: WTSEL, timing setting for debug purpose, default is 2'b01 • [10]: VS, timing setting for debug purpose, default is 1'b1 • [11]: VG, timing setting for debug purpose, default is 1'b1
[23:12]	u0_cdns_spdif_SCFG_sram_config	WR	0xd54	SRAM/ROM configuration. • [12]: SLP, sleep enable, high active, default is low. • [13]: SD, shutdown enable, high active, default is low. • [15:14]: RTSEL, timing setting for debug purpose, default is 2'b01 • [17:16]: PTSEL, timing setting for debug purpose, default is 2'b01 • [19:18]: TRB, timing setting for debug purpose, default is 2'b01 • [21:20]: WTSEL, timing setting for debug purpose, default is 2'b01 • [22]: VS, timing setting for debug purpose, default is 1'b1 • [23]: VG, timing setting for debug purpose, default is 1'b1
[24]	u0_cdns_spdif_trmodeo	RO	0x0	1 for transmitter 0 for receiver
[25]	u0_i2c_ic_en	RO	0x0	I2C interface enable.
[30:26]	u0_sdio_data_strobe_phase_ctrl	WR	0x0	data strobe delay chain select
[31]	u0_sdio_hbig_endian	WR	0x0	AHB bus interface endianness: • 1: Big-endian AHB bus interface • 0: Little-endian AHB bus interface

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SYS SYSCONSAIF SYSCFG 24

Table 2-301 SYS SYSCONSAIF SYSCFG 24 Register Description

Offset	0x18			
Default	0x4dea80			
Bit	Name	Access	Default	Description
[0]	u0_sdio_m_hbig_endian	WR	0x0	AHB master bus interface endianness: • 1: Big-endian AHB bus interface • 0: Little-endian AHB bus interface
[1]	u0_i2srx_3ch_adc_ena	WR	0x0	
[2]	u0_intmem_rom_sram_SCFG_-disable_rom	WR	0x0	
[14:3]	u0_intmem_rom_sram_sram_-config	WR	0xd50	SRAM/ROM configuration. • [3]: SLP, sleep enable, high active, default is low. • [4]: SD, shutdown enable, high active, default is low. • [6:5]: RTSEL, timing setting for debug purpose, default is 2'b00 • [8:7]: PTSEL, timing setting for debug purpose, default is 2'b01 • [10:9]: TRB, timing setting for debug purpose, default is 2'b01 • [12:11]: WTSEL, timing setting for debug purpose, default is 2'b01 • [13]: VS, timing setting for debug purpose, default is 1'b1 • [14]: VG, timing setting for debug purpose, default is 1'b1
[15]	u0_jtag_daisy_chain_jtag_en_0	WR	0x1	
[16]	u0_jtag_daisy_chain_jtag_en_1	WR	0x1	
[17]	u0_pdrstn_split_sw_usbpipe_-plugen	WR	0x0	
[20:18]	u0_pll_wrap_pll0_cpi_bias	WR	0x3	
[23:21]	u0_pll_wrap_pll0_cpp_bias	WR	0x2	
[24]	u0_pll_wrap_pll0_dacpd	WR	0x0	
[25]	u0_pll_wrap_pll0_dsmpd	WR	0x0	
[31:26]	Reserved	None	0x0	Reserved

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SYS SYSCONSAIF SYSCFG 28

Table 2-302 SYS SYSCONSAIF SYSCFG 28 Register Description

Offset	0x1c			
Default	0x53			
Bit	Name	Access	Default	Description
[0:11]	u0_pll_wrap_pll0_fbdiv	WR	0x53	
[31:12]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 32

Table 2-303 SYS SYSCONSAIF SYSCFG 32 Register Description

Offset	0x20			
Default	0x51555555			
Bit	Name	Access	Default	Description
[0:23]	u0_pll_wrap_pll0_frac	WR	0x555555	
[25:24]	u0_pll_wrap_pll0_gvco_bias	WR	0x1	
[26]	u0_pll_wrap_pll0_lock	RO	0x0	
[27]	u0_pll_wrap_pll0_pd	WR	0x0	
[29:28]	u0_pll_wrap_pll0_postdiv1	WR	0x1	
[30:31]	u0_pll_wrap_pll0_postdiv2	WR	0x1	

SYS SYSCONSAIF SYSCFG 36

Table 2-304 SYS SYSCONSAIF SYSCFG 36 Register Description

Offset	0x24			
Default	0xb02601			
Bit	Name	Access	Default	Description
[5:0]	u0_pll_wrap_pll0_prediv	WR	0x1	
[6]	u0_pll_wrap_pll0_testen	WR	0x0	
[8:7]	u0_pll_wrap_pll0_testsel	WR	0x0	
[11:9]	u0_pll_wrap_pll1_cpi_bias	WR	0x3	
[14:12]	u0_pll_wrap_pll1_cpp_bias	WR	0x2	
[15]	u0_pll_wrap_pll1_dacpd	WR	0x0	
[16]	u0_pll_wrap_pll1_dsmpd	WR	0x0	
[28:17]	u0_pll_wrap_pll1_fbdiv	WR	0x58	
[31:29]	Reserved	None	0x0	Reserved

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SYS SYSCONSAIF SYSCFG 40

Table 2-305 SYS SYSCONSAIF SYSCFG 40 Register Description

Offset	0x28			
Default	0x51e00000			
Bit	Name	Access	Default	Description
[0:23]	u0_pll_wrap_pll1_frac	WR	0xe00000	
[25:24]	u0_pll_wrap_pll1_gvco_bias	WR	0x1	
[26]	u0_pll_wrap_pll1_lock	RO	0x0	
[27]	u0_pll_wrap_pll1_pd	WR	0x0	
[29:28]	u0_pll_wrap_pll1_postdiv1	WR	0x1	
[30:31]	u0_pll_wrap_pll1_postdiv2	WR	0x1	

SYS SYSCONSAIF SYSCFG 44

Table 2-306 SYS SYSCONSAIF SYSCFG 44 Register Description

Offset	0x2c			
Default	0x662601			
Bit	Name	Access	Default	Description
[5:0]	u0_pll_wrap_pll1_prediv	WR	0x1	
[6]	u0_pll_wrap_pll1_testen	WR	0x0	
[8:7]	u0_pll_wrap_pll1_testsel	WR	0x0	
[11:9]	u0_pll_wrap_pll2_cpi_bias	WR	0x3	
[14:12]	u0_pll_wrap_pll2_cpp_bias	WR	0x2	
[15]	u0_pll_wrap_pll2_dacpd	WR	0x0	
[16]	u0_pll_wrap_pll2_dsmpd	WR	0x0	
[28:17]	u0_pll_wrap_pll2_fbdiv	WR	0x33	
[31:29]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 48

Table 2-307 SYS SYSCONSAIF SYSCFG 48 Register Description

Offset	0x30			
Default	0x41333333			
Bit	Name	Access	Default	Description
[0:23]	u0_pll_wrap_pll2_frac	WR	0x333333	
[25:24]	u0_pll_wrap_pll2_gvco_bias	WR	0x1	
[26]	u0_pll_wrap_pll2_lock	RO	0x0	
[27]	u0_pll_wrap_pll2_pd	WR	0x0	

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Table 2-307 SYS SYSCONSAIF SYSCFG 48 Register Description (continued)

Offset	0x30			
Default	**0x41333333**			
Bit	**Name**	**Access**	**Default**	**Description**
[29:28]	u0_pll_wrap_pll2_postdiv1	WR	0x0	
[30:31]	u0_pll_wrap_pll2_postdiv2	WR	0x1	

SYS SYSCONSAIF SYSCFG 52

Table 2-308 SYS SYSCONSAIF SYSCFG 52 Register Description

Offset	0x34			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	u0_pll_wrap_pll2_prediv	WR	0x1	
[6]	u0_pll_wrap_pll2_testen	WR	0x0	
[8:7]	u0_pll_wrap_pll2_testsel	WR	0x0	
[9]	u0_pll_wrap_syscfg_test_pll_-mode	WR	0x0	PLL test mode, only used for PLL BIST through jtag2apb.
[17:10]	u0_saif_audio_sdin_mux_-SCFG_i2sdin_sel	WR	0x0	
[18]	u0_sft7110_noc_bus_CLOCK_-GATING_OFF	WR	0x0	
[19]	u0_sft7110_noc_bus_oic_eve-mon_0_start	WR	0x0	
[20]	u0_sft7110_noc_bus_oic_eve-mon_0_trigger	RO	0x0	
[21]	u0_sft7110_noc_bus_oic_eve-mon_1_start	WR	0x0	
[22]	u0_sft7110_noc_bus_oic_eve-mon_1_trigger	RO	0x0	
[23]	u0_sft7110_noc_bus_oic_eve-mon_2_start	WR	0x0	
[24]	u0_sft7110_noc_bus_oic_eve-mon_2_trigger	RO	0x0	
[25]	u0_sft7110_noc_bus_oic_eve-mon_3_start	WR	0x0	
[26]	u0_sft7110_noc_bus_oic_eve-mon_3_trigger	RO	0x0	
[27]	u0_sft7110_noc_bus_oic_eve-mon_4_start	WR	0x0	
[28]	u0_sft7110_noc_bus_oic_eve-mon_4_trigger	RO	0x0	

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Table 2-308 SYS SYSCONSAIF SYSCFG 52 Register Description (continued)

Offset	0x34			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[29]	u0_sft7110_noc_bus_oic_evemon_5_start	WR	0x0	
[30]	u0_sft7110_noc_bus_oic_evemon_5_trigger	RO	0x0	
[31]	u0_sft7110_noc_bus_oic_evemon_6_start	WR	0x0	

SYS SYSCONSAIF SYSCFG 56

Table 2-309 SYS SYSCONSAIF SYSCFG 56 Register Description

Offset	0x38			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	u0_sft7110_noc_bus_oic_evemon_6_trigger	RO	0x0	
[1]	u0_sft7110_noc_bus_oic_evemon_7_start	WR	0x0	
[2]	u0_sft7110_noc_bus_oic_evemon_7_trigger	RO	0x0	
[3]	u0_sft7110_noc_bus_oic_evemon_8_start	WR	0x0	
[4]	u0_sft7110_noc_bus_oic_evemon_8_trigger	RO	0x0	
[5]	u0_sft7110_noc_bus_oic_ignore_modifiable_0	WR	0x0	
[6]	u0_sft7110_noc_bus_oic_ignore_modifiable_1	WR	0x0	
[7]	u0_sft7110_noc_bus_oic_ignore_modifiable_2	WR	0x0	
[8]	u0_sft7110_noc_bus_oic_ignore_modifiable_3	WR	0x0	
[9]	u0_sft7110_noc_bus_oic_ignore_modifiable_4	WR	0x0	
[10:31]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 60

Table 2-310 SYS SYSCONSAIF SYSCFG 60 Register Description

Offset	0x3c			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_threshold_0	WR	0x0	

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SYS SYSCONSAIF SYSCFG 64

Table 2-311 SYS SYSCONSAIF SYSCFG 64 Register Description

Offset	0x40			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_-threshold_1	WR	0x0	

SYS SYSCONSAIF SYSCFG 68

Table 2-312 SYS SYSCONSAIF SYSCFG 68 Register Description

Offset	0x44			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_-threshold_2	WR	0x0	

SYS SYSCONSAIF SYSCFG 72

Table 2-313 SYS SYSCONSAIF SYSCFG 72 Register Description

Offset	0x48			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_-threshold_3	WR	0x0	

SYS SYSCONSAIF SYSCFG 76

Table 2-314 SYS SYSCONSAIF SYSCFG 76 Register Description

Offset	0x4c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_-threshold_4	WR	0x0	

SYS SYSCONSAIF SYSCFG 80

Table 2-315 SYS SYSCONSAIF SYSCFG 80 Register Description

Offset	0x50			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_-threshold_5	WR	0x0	

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SYS SYSCONSAIF SYSCFG 84

Table 2-316 SYS SYSCONSAIF SYSCFG 84 Register Description

Offset	0x54			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_-threshold_6	WR	0x0	

SYS SYSCONSAIF SYSCFG 88

Table 2-317 SYS SYSCONSAIF SYSCFG 88 Register Description

Offset	0x58			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_-threshold_7	WR	0x0	

SYS SYSCONSAIF SYSCFG 92

Table 2-318 SYS SYSCONSAIF SYSCFG 92 Register Description

Offset	0x5c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_sft7110_noc_bus_oic_qch_clock_stop_-threshold_8	WR	0x0	

SYS SYSCONSAIF SYSCFG 96

Table 2-319 SYS SYSCONSAIF SYSCFG 96 Register Description

Offset	0x60			
Default	0x0			
Bit	Name	Access	Default	Description
[0]	u0_tdm16slot_CLKPOL	RO	0x0	
[1]	u0_tdm16slot_PCM_MS	RO	0x0	
[6:2]	u0_trace_mtx_SCFG_c0_in0_ctl	WR	0x0	
[11:7]	u0_trace_mtx_SCFG_c0_in1_ctl	WR	0x0	
[16:12]	u0_trace_mtx_SCFG_c1_in0_ctl	WR	0x0	
[21:17]	u0_trace_mtx_SCFG_c1_in1_ctl	WR	0x0	
[26:22]	u0_trace_mtx_SCFG_c2_in0_ctl	WR	0x0	
[31:27]	u0_trace_mtx_SCFG_c2_in1_ctl	WR	0x0	

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SYS SYSCONSAIF SYSCFG 100

Table 2-320 SYS SYSCONSAIF SYSCFG 100 Register Description

Offset	0x64			
Default	0x0			
Bit	Name	Access	Default	Description
[4:0]	u0_trace_mtx_SCFG_c3_in0_ctl	WR	0x0	
[9:5]	u0_trace_mtx_SCFG_c3_in1_ctl	WR	0x0	
[14:10]	u0_trace_mtx_SCFG_c4_in0_ctl	WR	0x0	
[19:15]	u0_trace_mtx_SCFG_c4_in1_ctl	WR	0x0	
[20]	u0_u7mc_sft7110_cease_from_tile_0	RO	0x0	
[21]	u0_u7mc_sft7110_cease_from_tile_1	RO	0x0	
[22]	u0_u7mc_sft7110_cease_from_tile_2	RO	0x0	
[23]	u0_u7mc_sft7110_cease_from_tile_3	RO	0x0	
[24]	u0_u7mc_sft7110_cease_from_tile_4	RO	0x0	
[25]	u0_u7mc_sft7110_halt_from_tile_0	RO	0x0	
[26]	u0_u7mc_sft7110_halt_from_tile_1	RO	0x0	
[27]	u0_u7mc_sft7110_halt_from_tile_2	RO	0x0	
[28]	u0_u7mc_sft7110_halt_from_tile_3	RO	0x0	
[29]	u0_u7mc_sft7110_halt_from_tile_4	RO	0x0	
[30:31]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 104

Table 2-321 SYS SYSCONSAIF SYSCFG 104 Register Description

Offset	0x68			
Default	0x2a000000			
Bit	Name	Access	Default	Description
[0:31]	u0_u7mc_sft7110_reset_vector_1_31_0_	WR	0x2a000000	

SYS SYSCONSAIF SYSCFG 108

Table 2-322 SYS SYSCONSAIF SYSCFG 108 Register Description

Offset	0x6c			
Default	0x0			
Bit	Name	Access	Default	Description
[3:0]	u0_u7mc_sft7110_reset_vector_1_35_32_	WR	0x0	
[4:31]	Reserved	None	0x0	Reserved

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SYS SYSCONSAIF SYSCFG 112

Table 2-323 SYS SYSCONSAIF SYSCFG 112 Register Description

Offset	0x70			
Default	0x2a000000			
Bit	Name	Access	Default	Description
[0:31]	u0_u7mc_sft7110_reset_vector_2_31_0_	WR	0x2a000000	

SYS SYSCONSAIF SYSCFG 116

Table 2-324 SYS SYSCONSAIF SYSCFG 116 Register Description

Offset	0x74			
Default	0x0			
Bit	Name	Access	Default	Description
[3:0]	u0_u7mc_sft7110_reset_vector_2_35_32_	WR	0x0	
[4:31]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 120

Table 2-325 SYS SYSCONSAIF SYSCFG 120 Register Description

Offset	0x78			
Default	0x2a000000			
Bit	Name	Access	Default	Description
[0:31]	u0_u7mc_sft7110_reset_vector_3_31_0_	WR	0x2a000000	

SYS SYSCONSAIF SYSCFG 124

Table 2-326 SYS SYSCONSAIF SYSCFG 124 Register Description

Offset	0x7c			
Default	0x0			
Bit	Name	Access	Default	Description
[3:0]	u0_u7mc_sft7110_reset_vector_3_35_32_	WR	0x0	
[4:31]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 128

Table 2-327 SYS SYSCONSAIF SYSCFG 128 Register Description

Offset	0x80			
Default	0x2a000000			
Bit	Name	Access	Default	Description
[0:31]	u0_u7mc_sft7110_reset_vector_4_31_0_	WR	0x2a000000	

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SYS SYSCONSAIF SYSCFG 132

Table 2-328 SYS SYSCONSAIF SYSCFG 132 Register Description

Offset	0x84			
Default	0x1aa8000			
Bit	Name	Access	Default	Description
[3:0]	u0_u7mc_sft7110_reset_vector_4_35_32_	WR	0x0	
[4]	u0_u7mc_sft7110_suppress_fetch_1	WR	0x0	
[5]	u0_u7mc_sft7110_suppress_fetch_2	WR	0x0	
[6]	u0_u7mc_sft7110_suppress_fetch_3	WR	0x0	
[7]	u0_u7mc_sft7110_suppress_fetch_4	WR	0x0	
[8]	u0_u7mc_sft7110_wfi_from_tile_0	RO	0x0	
[9]	u0_u7mc_sft7110_wfi_from_tile_1	RO	0x0	
[10]	u0_u7mc_sft7110_wfi_from_tile_2	RO	0x0	
[11]	u0_u7mc_sft7110_wfi_from_tile_3	RO	0x0	
[12]	u0_u7mc_sft7110_wfi_from_tile_4	RO	0x0	
[24:13]	u0_vdec_intsram_sram_config	WR	0xd54	SRAM/ROM configuration. • [13]: SLP, sleep enable, high active, default is low. • [14]: SD, shutdown enable, high active, default is low. • [16:15]: RTSEL, timing setting for debug purpose, default is 2'b01 • [18:17]: PTSEL, timing setting for debug purpose, default is 2'b01 • [20:19]: TRB, timing setting for debug purpose, default is 2'b01 • [22:21]: WTSEL, timing setting for debug purpose, default is 2'b01 • [23]: VS, timing setting for debug purpose, default is 1'b1 • [24]: VG, timing setting for debug purpose, default is 1'b1
[31:25]	Reserved	None	0x0	Reserved

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SYS SYSCONSAIF SYSCFG 136

Table 2-329 SYS SYSCONSAIF SYSCFG 136 Register Description

Offset	0x88			
Default	0xd54			
Bit	Name	Access	Default	Description
[0:11]	u0_venc_intsram_sram_config	WR	0xd54	SRAM/ROM configuration. • [0]: SLP, sleep enable, high active, default is low. • [1]: SD, shutdown enable, high active, default is low. • [2:3]: RTSEL, timing setting for debug purpose, default is 2'b01 • [4:5]: PTSEL, timing setting for debug purpose, default is 2'b01 • [6:7]: TRB, timing setting for debug purpose, default is 2'b01 • [8:9]: WTSEL, timing setting for debug purpose, default is 2'b01 • [10]: VS, timing setting for debug purpose, default is 1'b1 • [11]: VG, timing setting for debug purpose, default is 1'b1
[14:12]	u0_wave420l_i_ipu_current_buffer	WR	0x0	This signal indicates which buffer is currently active so that the VPU can correctly use the ipu_end_of_row signal for row counter.
[15]	u0_wave420l_i_ipu_end_of_row	WR	0x0	This signal is flipped every time when the IPU completes writing a row.
[16]	u0_wave420l_i_ipu_new_frame	WR	0x0	This signal is flipped every time the IPU starts writing a new frame.
[17]	u0_wave420l_o_vpu_idle	RO	0x0	VPU monitoring signal, This signal gives out an opposite value of VPU_BUSY register.
[18]	u1_can_ctrl_can_fd_enable	WR	0x0	
[19]	u1_can_ctrl_host_ecc_disable	WR	0x0	
[31:20]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 140

Table 2-330 SYS SYSCONSAIF SYSCFG 140 Register Description

Offset	0x8c			
Default	0x6aa00000			
Bit	Name	Access	Default	Description
[18:0]	u1_can_ctrl_host_if	RO	0x0	

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Table 2-330 SYS SYSCONSAIF SYSCFG 140 Register Description (continued)

Offset	0x8c			
Default	0x6aa00000			
Bit	Name	Access	Default	Description
[30:19]	u1_gmac5_axi64_SCFG_ram_cfg	WR	0xd54	SRAM/ROM configuration. • [19]: SLP, sleep enable, high active, default is low. • [20]: SD, shutdown enable, high active, default is low. • [22:21]: RTSEL, timing setting for debug purpose, default is 2'b01 • [24:23]: PTSEL, timing setting for debug purpose, default is 2'b01 • [25:26]: TRB, timing setting for debug purpose, default is 2'b01 • [27:28]: WTSEL, timing setting for debug purpose, default is 2'b01 • [29]: VS, timing setting for debug purpose, default is 1'b1 • [30]: VG, timing setting for debug purpose, default is 1'b1
[31]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 144

Table 2-331 SYS SYSCONSAIF SYSCFG 144 Register Description

Offset	0x90			
Default	0x4			
Bit	Name	Access	Default	Description
[1:0]	u1_gmac5_axi64_mac_-speed_o	RO	0x0	
[4:2]	u1_gmac5_axi64_phy_intf_sel_i	WR	0x1	Active PHY Selected When you have multiple GMAC PHY interfaces in your configuration, this field indicates the sampled value of the PHY selector during reset de-assertion. Values: • 0x0(GMII_MII): GMII or MII • 0x1(RGMII): RGMII • 0x2(SGMII): SGMII • 0x3(TBI): TBI • 0x4(RMII): RMII • 0x5(RTBI): RTBI

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Table 2-331 SYS SYSCONSAIF SYSCFG 144 Register Description (continued)

Offset	0x90			
Default	**0x4**			
Bit	**Name**	**Access**	**Default**	**Description**
				• 0x6(SMII): SMII • 0x7(REVMIII): RevMII
[31:5]	Reserved	None	0x0	Reserved

SYS SYSCONSAIF SYSCFG 148

Table 2-332 SYS SYSCONSAIF SYSCFG 148 Register Description

Offset	0x94			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u1_gmac5_axi64_ptp_timestamp_o_31_0_	RO	0x0	

SYS SYSCONSAIF SYSCFG 152

Table 2-333 SYS SYSCONSAIF SYSCFG 152 Register Description

Offset	0x98			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u1_gmac5_axi64_ptp_timestamp_o_63_32_	RO	0x0	

SYS SYSCONSAIF SYSCFG 156

Table 2-334 SYS SYSCONSAIF SYSCFG 156 Register Description

Offset	0x9c			
Default	**0x400**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	u1_i2c_ic_en	RO	0x0	I2C interface enable.
[5:1]	u1_sdio_data_strobe_phase_ctrl	WR	0x0	data strobe delay chain select
[6]	u1_sdio_hbig_endian	WR	0x0	AHB bus interface endianness: • 1: Big-endian AHB bus interface • 0: Little-endian AHB bus interface
[7]	u1_sdio_m_hbig_endian	WR	0x0	AHB master bus interface endianness: • 1: Big-endian AHB bus interface • 0: Little-endian AHB bus interface
[8]	u1_reset_ctrl_clr_reset_status	WR	0x0	
[9]	u1_reset_ctrl_pll_timecnt_finish	RO	0x0	

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Table 2-334 SYS SYSCONSAIF SYSCFG 156 Register Description (continued)

Offset	0x9c			
Default	**0x400**			
Bit	**Name**	**Access**	**Default**	**Description**
[10]	u1_reset_ctrl_rstn_sw	WR	0x1	
[14:11]	u1_reset_ctrl_sys_reset_status	RO	0x0	
[15]	u2_i2c_ic_en	RO	0x0	I2C interface enable.
[16]	u3_i2c_ic_en	RO	0x0	I2C interface enable.
[17]	u4_i2c_ic_en	RO	0x0	I2C interface enable.
[18]	u5_i2c_ic_en	RO	0x0	I2C interface enable.
[19]	u6_i2c_ic_en	RO	0x0	I2C interface enable.
[31:20]	Reserved	None	0x0	Reserved

2.8.5. STG SYSCON

The JH-7110 system provides the following STG SYSCON control registers which provides clock and reset signals to interfaces with master and/or slave signals.

SYS_SYSCONSAIF__SYSCFG_0

Table 2-335 SYS_SYSCONSAIF__SYSCFG_0 Register Description

Offset	0x0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0:3]	SCFG_hprot_sd0	WR	0x0	
[4:7]	SCFG_hprot_sd1	WR	0x0	
[8]	u0_cdn_usb_adp_en	RO	0x0	
[9]	u0_cdn_usb_adp_probe_ana	WR	0x0	
[10]	u0_cdn_usb_adp_probe_en	RO	0x0	
[11]	u0_cdn_usb_adp_sense_ana	WR	0x0	
[12]	u0_cdn_usb_adp_sense_en	RO	0x0	
[13]	u0_cdn_usb_adp_sink_current_en	RO	0x0	
[14]	u0_cdn_usb_adp_source_current_en	RO	0x0	
[15]	u0_cdn_usb_bc_en	RO	0x0	
[16]	u0_cdn_usb_chrg_vbus	WR	0x0	
[17]	u0_cdn_usb_dcd_comp_sts	WR	0x0	
[18]	u0_cdn_usb_dischrg_vbus	WR	0x0	
[19]	u0_cdn_usb_dm_vdat_ref_comp_en	RO	0x0	

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Table 2-335 SYS_SYSCONSAIF__SYSCFG_0 Register Description (continued)

Offset	0x0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[20]	u0_cdn_usb_dm_vdat_ref_comp_sts	WR	0x0	
[21]	u0_cdn_usb_dm_vlgc_comp_en	RO	0x0	
[22]	u0_cdn_usb_dm_vlgc_comp_sts	WR	0x0	
[23]	u0_cdn_usb_dp_vdat_ref_comp_en	RO	0x0	
[24]	u0_cdn_usb_dp_vdat_ref_comp_sts	WR	0x0	
[25]	u0_cdn_usb_host_system_err	WR	0x0	
[26]	u0_cdn_usb_hsystem_err_ext	RO	0x0	
[27]	u0_cdn_usb_idm_sink_en	RO	0x0	
[28]	u0_cdn_usb_idp_sink_en	RO	0x0	
[29]	u0_cdn_usb_idp_src_en	RO	0x0	
[30:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 4

Table 2-336 STG SYSCONSAIF SYSCFG 4 Register Description

Offset	0x4			
Default	**0x2000**			
Bit	**Name**	**Access**	**Default**	**Description**
[0:11]	u0_cdn_usb_lowest_belt	RO	0x0	LTM interface to software
[12]	u0_cdn_usb_ltm_host_req	RO	0x0	LTM interface to software
[13]	u0_cdn_usb_ltm_host_req_halt	WR	0x1	LTM interface to software
[14]	u0_cdn_usb_mdctrl_clk_sel	WR	0x0	
[15]	u0_cdn_usb_mdctrl_clk_status	RO	0x0	
[18:16]	u0_cdn_usb_mode_strap	WR	0x0	Can only be changed when pwrup_rst_n is low
[19]	u0_cdn_usb_otg_suspendm	WR	0x0	
[20]	u0_cdn_usb_otg_suspendm_byps	WR	0x0	
[21]	u0_cdn_usb_phy_bvalid	RO	0x0	
[22]	u0_cdn_usb_pll_en	WR	0x0	
[23]	u0_cdn_usb_refclk_mode	WR	0x0	
[24]	u0_cdn_usb_rid_a_comp_sts	WR	0x0	

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Table 2-336 STG SYSCONSAIF SYSCFG 4 Register Description (continued)

Offset	0x4			
Default	0x2000			
Bit	Name	Access	Default	Description
[25]	u0_cdn_usb_rid_b_comp_sts	WR	0x0	
[26]	u0_cdn_usb_rid_c_comp_sts	WR	0x0	
[27]	u0_cdn_usb_rid_float_comp_en	RO	0x0	
[28]	u0_cdn_usb_rid_float_comp_sts	WR	0x0	
[29]	u0_cdn_usb_rid_gnd_comp_sts	WR	0x0	
[30]	u0_cdn_usb_rid_nonfloat_comp_en	RO	0x0	
[31]	u0_cdn_usb_rx_dm	RO	0x0	

STG SYSCONSAIF SYSCFG 8

Table 2-337 STG SYSCONSAIF SYSCFG 8 Register Description

Offset	0x8			
Default	0x41000			
Bit	Name	Access	Default	Description
[0]	u0_cdn_usb_rx_dp	RO	0x0	
[1]	u0_cdn_usb_rx_rcv	RO	0x0	
[2]	u0_cdn_usb_self_test	WR	0x0	for software bist_test
[3]	u0_cdn_usb_sessend	RO	0x0	
[4]	u0_cdn_usb_sessvalid	RO	0x0	
[5]	u0_cdn_usb_sof	RO	0x0	
[6]	u0_cdn_usb_test_bist	RO	0x0	for software bist_test
[7]	u0_cdn_usb_usbdev_main_power_off_ack	RO	0x0	
[8]	u0_cdn_usb_usbdev_main_power_off_ready	RO	0x0	
[9]	u0_cdn_usb_usbdev_main_power_off_req	WR	0x0	
[10]	u0_cdn_usb_usbdev_main_power_on_ready	RO	0x0	
[11]	u0_cdn_usb_usbdev_main_power_on_req	RO	0x0	
[12]	u0_cdn_usb_usbdev_main_power_on_valid	WR	0x1	
[13]	u0_cdn_usb_usbdev_power_off_ack	RO	0x0	
[14]	u0_cdn_usb_usbdev_power_off_ready	RO	0x0	
[15]	u0_cdn_usb_usbdev_power_off_req	WR	0x0	
[16]	u0_cdn_usb_usbdev_power_on_ready	RO	0x0	
[17]	u0_cdn_usb_usbdev_power_on_req	RO	0x0	
[18]	u0_cdn_usb_usbdev_power_on_valid	WR	0x1	

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Table 2-337 STG SYSCONSAIF SYSCFG 8 Register Description (continued)

Offset	0x8			
Default	**0x41000**			
Bit	**Name**	**Access**	**Default**	**Description**
[19]	u0_cdn_usb_utmi_dmpulldown_sit	WR	0x0	
[20]	u0_cdn_usb_utmi_dppulldown_sit	WR	0x0	
[21]	u0_cdn_usb_utmi_fslsserialmode_sit	WR	0x0	
[22]	u0_cdn_usb_utmi_hostdisconnect_sit	RO	0x0	
[23]	u0_cdn_usb_utmi_iddig_sit	RO	0x0	
[24]	u0_cdn_usb_utmi_idpullup_sit	WR	0x0	
[25:26]	u0_cdn_usb_utmi_linestate_sit	RO	0x0	
[27:28]	u0_cdn_usb_utmi_opmode_sit	WR	0x0	
[29]	u0_cdn_usb_utmi_rxactive_sit	RO	0x0	
[30]	u0_cdn_usb_utmi_rxerror_sit	RO	0x0	
[31]	u0_cdn_usb_utmi_rxvalid_sit	RO	0x0	

STG SYSCONSAIF SYSCFG 12

Table 2-338 STG SYSCONSAIF SYSCFG 12 Register Description

Offset	0xc			
Default	**0x2**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	u0_cdn_usb_utmi_rxvalidh_sit	RO	0x0	
[1]	u0_cdn_usb_utmi_sessvld	WR	0x1	
[2]	u0_cdn_usb_utmi_termselect_sit	WR	0x0	
[3]	u0_cdn_usb_utmi_tx_dat_sit	WR	0x0	
[4]	u0_cdn_usb_utmi_tx_enable_n_sit	WR	0x0	
[5]	u0_cdn_usb_utmi_tx_se0_sit	WR	0x0	
[6]	u0_cdn_usb_utmi_txbitstuffenable_sit	WR	0x0	
[7]	u0_cdn_usb_utmi_txready_sit	RO	0x0	
[8]	u0_cdn_usb_utmi_txvalid_sit	WR	0x0	
[9]	u0_cdn_usb_utmi_txvalidh_sit	WR	0x0	
[10]	u0_cdn_usb_utmi_vbusvalid_sit	RO	0x0	
[12:11]	u0_cdn_usb_utmi_xcvrselect_sit	WR	0x0	
[13]	u0_cdn_usb_vdm_src_en	RO	0x0	
[14]	u0_cdn_usb_vdp_src_en	RO	0x0	
[15]	u0_cdn_usb_wakeup	WR	0x0	

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Table 2-338 STG SYSCONSAIF SYSCFG 12 Register Description (continued)

Offset	0xc			
Default	0x2			
Bit	Name	Access	Default	Description
[16]	u0_cdn_usb_xhc_d0_ack	RO	0x0	
[17]	u0_cdn_usb_xhc_d0_req	WR	0x0	
[18:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 16

Table 2-339 STG SYSCONSAIF SYSCFG 16 Register Description

Offset	0x10			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_cdn_usb_xhci_debug_bus	RO	0x0	

STG SYSCONSAIF SYSCFG 20

Table 2-340 STG SYSCONSAIF SYSCFG 20 Register Description

Offset	0x14			
Default	0x0			
Bit	Name	Access	Default	Description
[0:30]	u0_cdn_usb_xhci_debug_link_state	RO	0x0	
[31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 24

Table 2-341 STG SYSCONSAIF SYSCFG 24 Register Description

Offset	0x18			
Default	0x8200			
Bit	Name	Access	Default	Description
[4:0]	u0_cdn_usb_xhci_debug_sel	WR	0x0	
[5]	u0_cdn_usb_xhci_main_power_off_ack	RO	0x0	
[6]	u0_cdn_usb_xhci_main_power_off_req	WR	0x0	
[7]	u0_cdn_usb_xhci_main_power_on_ready	RO	0x0	
[8]	u0_cdn_usb_xhci_main_power_on_req	RO	0x0	
[9]	u0_cdn_usb_xhci_main_power_on_valid	WR	0x1	
[10]	u0_cdn_usb_xhci_power_off_ack	RO	0x0	
[11]	u0_cdn_usb_xhci_power_off_ready	RO	0x0	
[12]	u0_cdn_usb_xhci_power_off_req	WR	0x0	

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Table 2-341 STG SYSCONSAIF SYSCFG 24 Register Description (continued)

Offset	0x18			
Default	**0x8200**			
Bit	**Name**	**Access**	**Default**	**Description**
[13]	u0_cdn_usb_xhci_power_on_ready	RO	0x0	
[14]	u0_cdn_usb_xhci_power_on_req	RO	0x0	
[15]	u0_cdn_usb_xhci_power_on_valid	WR	0x1	
[16]	u0_e2_sft7110_cease_from_tile_0	RO	0x0	
[17]	u0_e2_sft7110_debug_from_tile_0	RO	0x0	
[18]	u0_e2_sft7110_halt_from_tile_0	RO	0x0	
[19:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 28

Table 2-342 STG SYSCONSAIF SYSCFG 28 Register Description

Offset	0x1c			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_e2_sft7110_nmi_0_rnmi_exception_vector	WR	0x0	

STG SYSCONSAIF SYSCFG 32

Table 2-343 STG SYSCONSAIF SYSCFG 32 Register Description

Offset	0x20			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_e2_sft7110_nmi_0_rnmi_interrupt_vector	WR	0x0	

STG SYSCONSAIF SYSCFG 36

Table 2-344 STG SYSCONSAIF SYSCFG 36 Register Description

Offset	0x24			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_e2_sft7110_reset_vector_0	WR	0x0	

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STG SYSCONSAIF SYSCFG 40

Table 2-345 STG SYSCONSAIF SYSCFG 40 Register Description

Offset	0x28			
Default	0x0			
Bit	Name	Access	Default	Description
[0]	u0_e2_sft7110_wfi_from_tile_0	RO	0x0	
[1:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 44

Table 2-346 STG SYSCONSAIF SYSCFG 44 Register Description

Offset	0x2c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_hifi4_AltResetVec	WR	0x0	Reset Vector Address

STG SYSCONSAIF SYSCFG 48

Table 2-347 STG SYSCONSAIF SYSCFG 48 Register Description

Offset	0x30			
Default	0x0			
Bit	Name	Access	Default	Description
[0]	u0_hifi4_BreakIn	WR	0x0	Debug signal
[1]	u0_hifi4_BreakInAck	RO	0x0	Debug signal
[2]	u0_hifi4_BreakOut	RO	0x0	Debug signal
[3]	u0_hifi4_BreakOutAck	WR	0x0	Debug signal
[4]	u0_hifi4_DebugMode	RO	0x0	Debug signal
[5]	u0_hifi4_DoubleExceptionError	RO	0x0	Fault Handling Signals
[6]	u0_hifi4_IRam0LoadStore	RO	0x0	indicates that iram0 work
[7]	u0_hifi4_IRam1LoadStore	RO	0x0	indicates that iram1 work
[8]	u0_hifi4_OCDHaltOnReset	WR	0x0	Debug signal
[9]	u0_hifi4_PFatalError	RO	0x0	Fault Handling Signals
[10:31]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 52

Table 2-348 STG SYSCONSAIF SYSCFG 52 Register Description

Offset	0x34			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_hifi4_PFaultInfo	RO	0x0	Fault Handling Signals

STG SYSCONSAIF SYSCFG 56

Table 2-349 STG SYSCONSAIF SYSCFG 56 Register Description

Offset	0x38			
Default	0x0			
Bit	Name	Access	Default	Description
[0]	u0_hifi4_PFaultInfoValid	RO	0x0	Fault Handling Signals
[16:1]	u0_hifi4_PRID	WR	0x0	module id
[17]	u0_hifi4_PWaitMode	RO	0x0	Wait Mode
[18]	u0_hifi4_RunStall	WR	0x0	Run Stall
[19:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 60

Table 2-350 STG SYSCONSAIF SYSCFG 60 Register Description

Offset	0x3c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_hifi4_SCFG_dsp_mst_offset	WR	0x0	• [0:11] indicates that master port remap address • [27:16] indicates that DMA port remap address

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STG SYSCONSAIF SYSCFG 64

Table 2-351 STG SYSCONSAIF SYSCFG 64 Register Description

Offset	0x40			
Default	0x40000000			
Bit	Name	Access	Default	Description
[0:31]	u0_hifi4_SCFG_dsp_slv_offset	WR	0x40000000	The value indicates the slave port remap address

STG SYSCONSAIF SYSCFG 68

Table 2-352 STG SYSCONSAIF SYSCFG 68 Register Description

Offset	0x44			
Default	0xd54			
Bit	Name	Access	Default	Description
[0:11]	u0_hifi4_SCFG_sram_config	WR	0xd54	SRAM/ROM configuration. • [0]: SLP, sleep enable, high active, default is low. • [1]: SD, shutdown enable, high active, default is low. • [2:3]: RTSEL, timing setting for debug purpose, default is 2'b01 • [4:5]: PTSEL, timing setting for debug purpose, default is 2'b01 • [6:7]: TRB, timing setting for debug purpose, default is 2'b01 • [8:9]: WTSEL, timing setting for debug purpose, default is 2'b01 • [10]: VS, timing setting for debug purpose, default is 1'b1 • [11]: VG, timing setting for debug purpose, default is 1'b1
[12]	u0_hifi4_StatVectorSel	WR	0x0	When the value is 1, it indicates that the AltResetVec is valid
[13]	u0_hifi4_TrigIn_iDMA	WR	0x0	DMA port trigger
[14]	u0_hifi4_TrigOut_iDMA	RO	0x0	DMA port trigger
[15]	u0_hifi4_XOCDMode	RO	0x0	Debug signal
[16]	u0_plda_pcie_align_detect	RO	0x0	
[31:17]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 72

Table 2-353 STG SYSCONSAIF SYSCFG 72 Register Description

Offset	0x48			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aratomop_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 76

Table 2-354 STG SYSCONSAIF SYSCFG 76 Register Description

Offset	0x4c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aratomop_63_32_	RO	0x0	

STG SYSCONSAIF SYSCFG 80

Table 2-355 STG SYSCONSAIF SYSCFG 80 Register Description

Offset	0x50			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aratomop_95_64_	RO	0x0	

STG SYSCONSAIF SYSCFG 84

Table 2-356 STG SYSCONSAIF SYSCFG 84 Register Description

Offset	0x54			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aratomop_127_96_	RO	0x0	

STG SYSCONSAIF SYSCFG 88

Table 2-357 STG SYSCONSAIF SYSCFG 88 Register Description

Offset	0x58			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aratomop_159_128_	RO	0x0	

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STG SYSCONSAIF SYSCFG 92

Table 2-358 STG SYSCONSAIF SYSCFG 92 Register Description

Offset	0x5c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aratomop_191_160_	RO	0x0	

STG SYSCONSAIF SYSCFG 96

Table 2-359 STG SYSCONSAIF SYSCFG 96 Register Description

Offset	0x60			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aratomop_223_192_	RO	0x0	

STG SYSCONSAIF SYSCFG 100

Table 2-360 STG SYSCONSAIF SYSCFG 100 Register Description

Offset	0x64			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aratomop_255_224_	RO	0x0	

STG SYSCONSAIF SYSCFG 104

Table 2-361 STG SYSCONSAIF SYSCFG 104 Register Description

Offset	0x68			
Default	0x0			
Bit	Name	Access	Default	Description
[1:0]	u0_plda_pcie_axi4_mst0_aratomop_257_256_	RO	0x0	
[16:2]	u0_plda_pcie_axi4_mst0_arfunc	RO	0x0	
[20:17]	u0_plda_pcie_axi4_mst0_arregion	RO	0x0	
[31:21]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 108

Table 2-362 STG SYSCONSAIF SYSCFG 108 Register Description

Offset	0x6c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_aruser_31_0_	RO	0x0	

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STG SYSCONSAIF SYSCFG 112

Table 2-363 STG SYSCONSAIF SYSCFG 112 Register Description

Offset	0x70			
Default	0x0			
Bit	Name	Access	Default	Description
[20:0]	u0_plda_pcie_axi4_mst0_aruser_52_32_	RO	0x0	
[31:21]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 116

Table 2-364 STG SYSCONSAIF SYSCFG 116 Register Description

Offset	0x74			
Default	0x0			
Bit	Name	Access	Default	Description
[14:0]	u0_plda_pcie_axi4_mst0_awfunc	RO	0x0	
[18:15]	u0_plda_pcie_axi4_mst0_awregion	RO	0x0	
[19:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 120

Table 2-365 STG SYSCONSAIF SYSCFG 120 Register Description

Offset	0x78			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_awuser_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 124

Table 2-366 STG SYSCONSAIF SYSCFG 124 Register Description

Offset	0x7c			
Default	0x0			
Bit	Name	Access	Default	Description
[10:0]	u0_plda_pcie_axi4_mst0_awuser_42_32_	RO	0x0	
[18:11]	u0_plda_pcie_axi4_mst0_rderr	WR	0x0	
[19:31]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 128

Table 2-367 STG SYSCONSAIF SYSCFG 128 Register Description

Offset	0x80			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_mst0_ruser	WR	0x0	

STG SYSCONSAIF SYSCFG 132

Table 2-368 STG SYSCONSAIF SYSCFG 132 Register Description

Offset	0x84			
Default	0x0			
Bit	Name	Access	Default	Description
[7:0]	u0_plda_pcie_axi4_mst0_wderr	RO	0x0	
[8:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 136

Table 2-369 STG SYSCONSAIF SYSCFG 136 Register Description

Offset	0x88			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aratomop_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 140

Table 2-370 STG SYSCONSAIF SYSCFG 140 Register Description

Offset	0x8c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aratomop_63_32_	WR	0x0	

STG SYSCONSAIF SYSCFG 144

Table 2-371 STG SYSCONSAIF SYSCFG 144 Register Description

Offset	0x90			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aratomop_95_64_	WR	0x0	

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STG SYSCONSAIF SYSCFG 148

Table 2-372 STG SYSCONSAIF SYSCFG 148 Register Description

Offset	0x94			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aratomop_127_96_	WR	0x0	

STG SYSCONSAIF SYSCFG 152

Table 2-373 STG SYSCONSAIF SYSCFG 152 Register Description

Offset	0x98			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aratomop_159_128_	WR	0x0	

STG SYSCONSAIF SYSCFG 156

Table 2-374 STG SYSCONSAIF SYSCFG 156 Register Description

Offset	0x9c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aratomop_191_160_	WR	0x0	

STG SYSCONSAIF SYSCFG 160

Table 2-375 STG SYSCONSAIF SYSCFG 160 Register Description

Offset	0xa0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aratomop_223_192_	WR	0x0	

STG SYSCONSAIF SYSCFG 164

Table 2-376 STG SYSCONSAIF SYSCFG 164 Register Description

Offset	0xa4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aratomop_255_224_	WR	0x0	

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STG SYSCONSAIF SYSCFG 168

Table 2-377 STG SYSCONSAIF SYSCFG 168 Register Description

Offset	0xa8			
Default	0x0			
Bit	Name	Access	Default	Description
[1:0]	u0_plda_pcie_axi4_slv0_aratomop_257_256_	WR	0x0	
[16:2]	u0_plda_pcie_axi4_slv0_arfunc	WR	0x0	
[20:17]	u0_plda_pcie_axi4_slv0_arregion	WR	0x0	
[31:21]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 172

Table 2-378 STG SYSCONSAIF SYSCFG 172 Register Description

Offset	0xac			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_aruser_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 176

Table 2-379 STG SYSCONSAIF SYSCFG 176 Register Description

Offset	0xb0			
Default	0x0			
Bit	Name	Access	Default	Description
[8:0]	u0_plda_pcie_axi4_slv0_aruser_40_32_	WR	0x0	
[23:9]	u0_plda_pcie_axi4_slv0_awfunc	WR	0x0	
[27:24]	u0_plda_pcie_axi4_slv0_awregion	WR	0x0	
[31:28]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 180

Table 2-380 STG SYSCONSAIF SYSCFG 180 Register Description

Offset	0xb4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_awuser_31_0_	WR	0x0	

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STG SYSCONSAIF SYSCFG 184

Table 2-381 STG SYSCONSAIF SYSCFG 184 Register Description

Offset	0xb8			
Default	0x0			
Bit	Name	Access	Default	Description
[8:0]	u0_plda_pcie_axi4_slv0_awuser_40_32_	WR	0x0	
[16:9]	u0_plda_pcie_axi4_slv0_rderr	RO	0x0	
[31:17]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 188

Table 2-382 STG SYSCONSAIF SYSCFG 188 Register Description

Offset	0xbc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_axi4_slv0_ruser	RO	0x0	

STG SYSCONSAIF SYSCFG 192

Table 2-383 STG SYSCONSAIF SYSCFG 192 Register Description

Offset	0xc0			
Default	0x0			
Bit	Name	Access	Default	Description
[7:0]	u0_plda_pcie_axi4_slv0_wderr	WR	0x0	
[22:8]	u0_plda_pcie_axi4_slvl_arfunc	WR	0x0	
[31:23]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 196

Table 2-384 STG SYSCONSAIF SYSCFG 196 Register Description

Offset	0xc4			
Default	0x0			
Bit	Name	Access	Default	Description
[14:0]	u0_plda_pcie_axi4_slvl_awfunc	WR	0x0	
[16:15]	u0_plda_pcie_bus_width_o	RO	0x0	
[17]	u0_plda_pcie_bypass_codec	WR	0x0	
[19:18]	u0_plda_pcie_ckref_src	WR	0x0	
[21:20]	u0_plda_pcie_clk_sel	WR	0x0	
[22]	u0_plda_pcie_clkreq	WR	0x0	
[31:23]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 200

Table 2-385 STG SYSCONSAIF SYSCFG 200 Register Description

Offset	0xc8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 204

Table 2-386 STG SYSCONSAIF SYSCFG 204 Register Description

Offset	0xcc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_63_32_	WR	0x0	

STG SYSCONSAIF SYSCFG 208

Table 2-387 STG SYSCONSAIF SYSCFG 208 Register Description

Offset	0xd0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_95_64_	WR	0x0	

STG SYSCONSAIF SYSCFG 212

Table 2-388 STG SYSCONSAIF SYSCFG 212 Register Description

Offset	0xd4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_127_96_	WR	0x0	

STG SYSCONSAIF SYSCFG 216

Table 2-389 STG SYSCONSAIF SYSCFG 216 Register Description

Offset	0xd8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_159_128_	WR	0x0	

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STG SYSCONSAIF SYSCFG 220

Table 2-390 STG SYSCONSAIF SYSCFG 220 Register Description

Offset	0xdc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_191_160_	WR	0x0	

STG SYSCONSAIF SYSCFG 224

Table 2-391 STG SYSCONSAIF SYSCFG 224 Register Description

Offset	0xe0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_223_192_	WR	0x0	

STG SYSCONSAIF SYSCFG 228

Table 2-392 STG SYSCONSAIF SYSCFG 228 Register Description

Offset	0xe4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_255_224_	WR	0x0	

STG SYSCONSAIF SYSCFG 232

Table 2-393 STG SYSCONSAIF SYSCFG 232 Register Description

Offset	0xe8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_287_256_	WR	0x0	

STG SYSCONSAIF SYSCFG 236

Table 2-394 STG SYSCONSAIF SYSCFG 236 Register Description

Offset	0xec			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_319_288_	WR	0x0	

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STG SYSCONSAIF SYSCFG 240

Table 2-395 STG SYSCONSAIF SYSCFG 240 Register Description

Offset	0xf0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_351_320_	WR	0x0	

STG SYSCONSAIF SYSCFG 244

Table 2-396 STG SYSCONSAIF SYSCFG 244 Register Description

Offset	0xf4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_383_352_	WR	0x0	

STG SYSCONSAIF SYSCFG 248

Table 2-397 STG SYSCONSAIF SYSCFG 248 Register Description

Offset	0xf8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_415_384_	WR	0x0	

STG SYSCONSAIF SYSCFG 252

Table 2-398 STG SYSCONSAIF SYSCFG 252 Register Description

Offset	0xfc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_447_416_	WR	0x0	

STG SYSCONSAIF SYSCFG 256

Table 2-399 STG SYSCONSAIF SYSCFG 256 Register Description

Offset	0x100			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_479_448_	WR	0x0	

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STG SYSCONSAIF SYSCFG 260

Table 2-400 STG SYSCONSAIF SYSCFG 260 Register Description

Offset	0x104			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_511_480_	WR	0x0	

STG SYSCONSAIF SYSCFG 264

Table 2-401 STG SYSCONSAIF SYSCFG 264 Register Description

Offset	0x108			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_543_512_	WR	0x0	

STG SYSCONSAIF SYSCFG 268

Table 2-402 STG SYSCONSAIF SYSCFG 268 Register Description

Offset	0x10c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_575_544_	WR	0x0	

STG SYSCONSAIF SYSCFG 272

Table 2-403 STG SYSCONSAIF SYSCFG 272 Register Description

Offset	0x110			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_607_576_	WR	0x0	

STG SYSCONSAIF SYSCFG 276

Table 2-404 STG SYSCONSAIF SYSCFG 276 Register Description

Offset	0x114			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_671_640_	WR	0x0	

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STG SYSCONSAIF SYSCFG 284

Table 2-405 STG SYSCONSAIF SYSCFG 284 Register Description

Offset	0x11c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_703_672_	WR	0x0	

STG SYSCONSAIF SYSCFG 288

Table 2-406 STG SYSCONSAIF SYSCFG 288 Register Description

Offset	0x120			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_735_704_	WR	0x0	

STG SYSCONSAIF SYSCFG 292

Table 2-407 STG SYSCONSAIF SYSCFG 292 Register Description

Offset	0x124			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_767_736_	WR	0x0	

STG SYSCONSAIF SYSCFG 296

Table 2-408 STG SYSCONSAIF SYSCFG 296 Register Description

Offset	0x128			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_799_768_	WR	0x0	

STG SYSCONSAIF SYSCFG 300

Table 2-409 STG SYSCONSAIF SYSCFG 300 Register Description

Offset	0x12c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_k_phyparam_831_800_	WR	0x0	

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STG SYSCONSAIF SYSCFG 304

Table 2-410 STG SYSCONSAIF SYSCFG 304 Register Description

Offset	0x130			
Default	0x0			
Bit	Name	Access	Default	Description
[7:0]	u0_plda_pcie_k_phyparam_839_832_	WR	0x0	
[8]	u0_plda_pcie_k_rp_nep	WR	0x0	
[9]	u0_plda_pcie_l1sub_entack	RO	0x0	
[10]	u0_plda_pcie_l1sub_entreq	WR	0x0	
[31:11]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 308

Table 2-411 STG SYSCONSAIF SYSCFG 308 Register Description

Offset	0x134			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_local_interrupt_in	WR	0x0	

STG SYSCONSAIF SYSCFG 312

Table 2-412 SYS_SYSCONSAIF__SYSCFG_0 Register Description

Offset	0x138			
Default	0x4800001			
Bit	Name	Access	Default	Description
[0]	u0_plda_pcie_mperstn	WR	0x1	
[1]	u0_plda_pcie_pcie_ebuf_mode	WR	0x0	
[24:2]	u0_plda_pcie_pcie_phy_test_cfg	WR	0x200000	
[25]	u0_plda_pcie_pcie_rx_eq_training	WR	0x0	
[26]	u0_plda_pcie_pcie_rxterm_en	WR	0x1	
[27]	u0_plda_pcie_pcie_tx_oneszeros	WR	0x0	
[31:28]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 316

Table 2-413 STG SYSCONSAIF SYSCFG 316 Register Description

Offset	0x13c			
Default	0x0			
Bit	Name	Access	Default	Description
[19:0]	u0_plda_pcie_pf0_offset	WR	0x0	

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Table 2-413 STG SYSCONSAIF SYSCFG 316 Register Description (continued)

Offset	0x13c			
Default	0x0			
Bit	Name	Access	Default	Description
[31:20]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 320

Table 2-414 STG SYSCONSAIF SYSCFG 320 Register Description

Offset	0x140			
Default	0x0			
Bit	Name	Access	Default	Description
[19:0]	u0_plda_pcie_pf1_offset	WR	0x0	
[31:20]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 324

Table 2-415 STG SYSCONSAIF SYSCFG 324 Register Description

Offset	0x144			
Default	0x0			
Bit	Name	Access	Default	Description
[19:0]	u0_plda_pcie_pf2_offset	WR	0x0	
[31:20]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 328

Table 2-416 STG SYSCONSAIF SYSCFG 328 Register Description

Offset	0x148			
Default	0x0			
Bit	Name	Access	Default	Description
[19:0]	u0_plda_pcie_pf3_offset	WR	0x0	
[21:20]	u0_plda_pcie_phy_mode	WR	0x0	
[22]	u0_plda_pcie_pl_clkrem_allow	WR	0x0	
[23]	u0_plda_pcie_pl_clkreq_oen	RO	0x0	
[25:24]	u0_plda_pcie_pl_equ_phase	RO	0x0	
[30:26]	u0_plda_pcie_pl_ltssm	RO	0x0	
[31]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 332

Table 2-417 STG SYSCONSAIF SYSCFG 332 Register Description

Offset	0x14c			
Default	0x0			
Bit	Name	Access	Default	Description
[4:0]	u0_plda_pcie_pl_pclk_rate	RO	0x0	
[31:5]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 336

Table 2-418 SYS_SYSCONSAIF__SYSCFG_0 Register Description

Offset	0x150			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_pl_sideband_in_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 340

Table 2-419 STG SYSCONSAIF SYSCFG 340 Register Description

Offset	0x154			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_pl_sideband_in_63_32_	WR	0x0	

STG SYSCONSAIF SYSCFG 344

Table 2-420 STG SYSCONSAIF SYSCFG 344 Register Description

Offset	0x158			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_pl_sideband_out_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 348

Table 2-421 STG SYSCONSAIF SYSCFG 348 Register Description

Offset	0x15c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_pl_sideband_out_63_32_	RO	0x0	

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STG SYSCONSAIF SYSCFG 352

Table 2-422 SYS_SYSCONSAIF__SYSCFG_0 Register Description

Offset	0x160			
Default	0x1			
Bit	Name	Access	Default	Description
[0]	u0_plda_pcie_pl_wake_in	WR	0x1	
[1]	u0_plda_pcie_pl_wake_oen	RO	0x0	
[2]	u0_plda_pcie_rx_standby_o	RO	0x0	
[31:3]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 356

Table 2-423 STG SYSCONSAIF SYSCFG 356 Register Description

Offset	0x164			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_in_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 360

Table 2-424 STG SYSCONSAIF SYSCFG 360 Register Description

Offset	0x168			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_in_63_32_	WR	0x0	

STG SYSCONSAIF SYSCFG 364

Table 2-425 STG SYSCONSAIF SYSCFG 364 Register Description

Offset	0x16c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 368

Table 2-426 STG SYSCONSAIF SYSCFG 368 Register Description

Offset	0x170			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_63_32_	RO	0x0	

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STG SYSCONSAIF SYSCFG 372

Table 2-427 STG SYSCONSAIF SYSCFG 372 Register Description

Offset	0x174			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_95_64_	RO	0x0	

STG SYSCONSAIF SYSCFG 376

Table 2-428 STG SYSCONSAIF SYSCFG 376 Register Description

Offset	0x178			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_127_96_	RO	0x0	

STG SYSCONSAIF SYSCFG 380

Table 2-429 STG SYSCONSAIF SYSCFG 380 Register Description

Offset	0x17c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_159_128_	RO	0x0	

STG SYSCONSAIF SYSCFG 384

Table 2-430 STG SYSCONSAIF SYSCFG 384 Register Description

Offset	0x180			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_191_160_	RO	0x0	

STG SYSCONSAIF SYSCFG 388

Table 2-431 STG SYSCONSAIF SYSCFG 388 Register Description

Offset	0x184			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_223_192_	RO	0x0	

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STG SYSCONSAIF SYSCFG 392

Table 2-432 STG SYSCONSAIF SYSCFG 392 Register Description

Offset	0x188			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_255_224_	RO	0x0	

STG SYSCONSAIF SYSCFG 396

Table 2-433 STG SYSCONSAIF SYSCFG 396 Register Description

Offset	0x18c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_287_256_	RO	0x0	

STG SYSCONSAIF SYSCFG 400

Table 2-434 STG SYSCONSAIF SYSCFG 400 Register Description

Offset	0x190			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_319_288_	RO	0x0	

STG SYSCONSAIF SYSCFG 404

Table 2-435 STG SYSCONSAIF SYSCFG 404 Register Description

Offset	0x198			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_383_352_	RO	0x0	

STG SYSCONSAIF SYSCFG 408

Table 2-436 STG SYSCONSAIF SYSCFG 408 Register Description

Offset	0x198			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_383_352_	RO	0x0	

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STG SYSCONSAIF SYSCFG 412

Table 2-437 STG SYSCONSAIF SYSCFG 412 Register Description

Offset	0x19c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_415_384_	RO	0x0	

STG SYSCONSAIF SYSCFG 416

Table 2-438 STG SYSCONSAIF SYSCFG 416 Register Description

Offset	0x1a0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_447_416_	RO	0x0	

STG SYSCONSAIF SYSCFG 420

Table 2-439 STG SYSCONSAIF SYSCFG 420 Register Description

Offset	0x1a4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_479_448_	RO	0x0	

STG SYSCONSAIF SYSCFG 424

Table 2-440 STG SYSCONSAIF SYSCFG 424 Register Description

Offset	0x1a8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_bridge_511_480_	RO	0x0	

STG SYSCONSAIF SYSCFG 428

Table 2-441 STG SYSCONSAIF SYSCFG 428 Register Description

Offset	0x1ac			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_31_0_	RO	0x0	

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STG SYSCONSAIF SYSCFG 432

Table 2-442 STG SYSCONSAIF SYSCFG 432 Register Description

Offset	0x1b0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_63_32_	RO	0x0	

STG SYSCONSAIF SYSCFG 436

Table 2-443 STG SYSCONSAIF SYSCFG 436 Register Description

Offset	0x1b0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_63_32_	RO	0x0	

STG SYSCONSAIF SYSCFG 440

Table 2-444 STG SYSCONSAIF SYSCFG 440 Register Description

Offset	0x1b8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_127_96_	RO	0x0	

STG SYSCONSAIF SYSCFG 444

Table 2-445 STG SYSCONSAIF SYSCFG 444 Register Description

Offset	0x1bc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_159_128_	RO	0x0	

STG SYSCONSAIF SYSCFG 448

Table 2-446 STG SYSCONSAIF SYSCFG 448 Register Description

Offset	0x1c0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_191_160_	RO	0x0	

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STG SYSCONSAIF SYSCFG 452

Table 2-447 STG SYSCONSAIF SYSCFG 452 Register Description

Offset	0x1c4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_223_192_	RO	0x0	

STG SYSCONSAIF SYSCFG 456

Table 2-448 STG SYSCONSAIF SYSCFG 456 Register Description

Offset	0x1c8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_255_224_	RO	0x0	

STG SYSCONSAIF SYSCFG 460

Table 2-449 STG SYSCONSAIF SYSCFG 460 Register Description

Offset	0x1cc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_287_256_	RO	0x0	

STG SYSCONSAIF SYSCFG 464

Table 2-450 STG SYSCONSAIF SYSCFG 464 Register Description

Offset	0x1d0			
Default	0x0			
Bit	Name	Access	Default	Description
31:0]	u0_plda_pcie_test_out_pcie_319_288_	RO	0x0	

STG SYSCONSAIF SYSCFG 468

Table 2-451 STG SYSCONSAIF SYSCFG 468 Register Description

Offset	0x1d4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_351_320_	RO	0x0	

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STG SYSCONSAIF SYSCFG 472

Table 2-452 STG SYSCONSAIF SYSCFG 472 Register Description

Offset	0x1d8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_383_352_	RO	0x0	

STG SYSCONSAIF SYSCFG 476

Table 2-453 STG SYSCONSAIF SYSCFG 476 Register Description

Offset	0x1dc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_415_384_	RO	0x0	

STG SYSCONSAIF SYSCFG 480

Table 2-454 STG SYSCONSAIF SYSCFG 480 Register Description

Offset	0x1e0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_447_416_	RO	0x0	

STG SYSCONSAIF SYSCFG 484

Table 2-455 STG SYSCONSAIF SYSCFG 484 Register Description

Offset	0x1e4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_479_448_	RO	0x0	

STG SYSCONSAIF SYSCFG 488

Table 2-456 STG SYSCONSAIF SYSCFG 488 Register Description

Offset	0x1e8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_plda_pcie_test_out_pcie_511_480_	RO	0x0	

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STG SYSCONSAIF SYSCFG 492

Table 2-457 STG SYSCONSAIF SYSCFG 492 Register Description

Offset	0x1ec			
Default	0xc80			
Bit	Name	Access	Default	Description
[0:3]	u0_plda_pcie_test_sel	WR	0x0	
[25:4]	u0_plda_pcie_tl_clock_freq	WR	0xc8	
[31:26]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 496

Table 2-458 STG SYSCONSAIF SYSCFG 496 Register Description

Offset	0x1f0			
Default	0x0			
Bit	Name	Access	Default	Description
[15:0]	u0_plda_pcie_tl_ctrl_hotplug	RO	0x0	
[31:16]	u0_plda_pcie_tl_report_hotplug	WR	0x0	

STG SYSCONSAIF SYSCFG 500

Table 2-459 STG SYSCONSAIF SYSCFG 500 Register Description

Offset	0x1f4			
Default	0x6aa008			
Bit	Name	Access	Default	Description
[1:0]	u0_plda_pcie_tx_pattern	WR	0x0	
[2:3]	u0_plda_pcie_usb3_bus_width	WR	0x2	
[4]	u0_plda_pcie_usb3_phy_enable	WR	0x0	
[6:5]	u0_plda_pcie_usb3_rate	WR	0x0	
[7]	u0_plda_pcie_usb3_rx_standby	WR	0x0	
[8]	u0_plda_pcie_xwdecerr	RO	0x0	
[9]	u0_plda_pcie_xwerrclr	WR	0x0	
[10]	u0_plda_pcie_xwslverr	RO	0x0	
[22:11]	u0_sec_top_sramcfg	WR	0xd54	SRAM/ROM configuration. • [11]: SLP, sleep enable, high active, default is low. • [12]: SD, shutdown enable, high active, default is low. • [14:13]: RTSEL, timing setting for debug purpose, default is 2’b01

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Table 2-459 STG SYSCONSAIF SYSCFG 500 Register Description (continued)

Offset	0x1f4			
Default	0x6aa008			
Bit	Name	Access	Default	Description
				• [16:15]: PTSEL, timing setting for debug purpose, default is 2'b01 • [18:17]: TRB, timing setting for debug purpose, default is 2'b01 • [20:19]: WTSEL, timing setting for debug purpose, default is 2'b01 • [21]: VS, timing setting for debug purpose, default is 1'b1 • [22]: VG, timing setting for debug purpose, default is 1'b1
[23]	u1_plda_pcie_align_detect	RO	0x0	
[31:24]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 504

Table 2-460 STG SYSCONSAIF SYSCFG 504 Register Description

Offset	0x1f8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aratomop_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 508

Table 2-461 STG SYSCONSAIF SYSCFG 508 Register Description

Offset	0x1fc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aratomop_63_32_	RO	0x0	

STG SYSCONSAIF SYSCFG 512

Table 2-462 STG SYSCONSAIF SYSCFG 512 Register Description

Offset	0x200			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aratomop_95_64_	RO	0x0	

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STG SYSCONSAIF SYSCFG 516

Table 2-463 STG SYSCONSAIF SYSCFG 516 Register Description

Offset	0x204			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aratomop_127_96_	RO	0x0	

STG SYSCONSAIF SYSCFG 520

Table 2-464 STG SYSCONSAIF SYSCFG 520 Register Description

Offset	0x208			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aratomop_159_128_	RO	0x0	

STG SYSCONSAIF SYSCFG 524

Table 2-465 STG SYSCONSAIF SYSCFG 524 Register Description

Offset	0x20c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aratomop_191_160_	RO	0x0	

STG SYSCONSAIF SYSCFG 528

Table 2-466 STG SYSCONSAIF SYSCFG 528 Register Description

Offset	0x210			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aratomop_223_192_	RO	0x0	

STG SYSCONSAIF SYSCFG 532

Table 2-467 STG SYSCONSAIF SYSCFG 532 Register Description

Offset	0x214			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aratomop_255_224_	RO	0x0	

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STG SYSCONSAIF SYSCFG 536

Table 2-468 STG SYSCONSAIF SYSCFG 536 Register Description

Offset	0x218			
Default	0x0			
Bit	Name	Access	Default	Description
[1:0]	u1_plda_pcie_axi4_mst0_aratomop_257_256_	RO	0x0	
[16:2]	u1_plda_pcie_axi4_mst0_arfunc	RO	0x0	
[20:17]	u1_plda_pcie_axi4_mst0_arregion	RO	0x0	
[31:21]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 540

Table 2-469 STG SYSCONSAIF SYSCFG 540 Register Description

Offset	0x21c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_aruser_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 544

Table 2-470 STG SYSCONSAIF SYSCFG 544 Register Description

Offset	0x220			
Default	0x0			
Bit	Name	Access	Default	Description
[20:0]	u1_plda_pcie_axi4_mst0_aruser_52_32_	RO	0x0	
[31:21]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 548

Table 2-471 STG SYSCONSAIF SYSCFG 548 Register Description

Offset	0x224			
Default	0x0			
Bit	Name	Access	Default	Description
[14:0]	u1_plda_pcie_axi4_mst0_awfunc	RO	0x0	
[18:15]	u1_plda_pcie_axi4_mst0_awregion	RO	0x0	
[19:31]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 552

Table 2-472 STG SYSCONSAIF SYSCFG 552 Register Description

Offset	0x228			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_awuser_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 556

Table 2-473 STG SYSCONSAIF SYSCFG 556 Register Description

Offset	0x22c			
Default	0x0			
Bit	Name	Access	Default	Description
[10:0]	u1_plda_pcie_axi4_mst0_awuser_42_32_	RO	0x0	
[18:11]	u1_plda_pcie_axi4_mst0_rderr	WR	0x0	
[19:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 560

Table 2-474 STG SYSCONSAIF SYSCFG 560 Register Description

Offset	0x230			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_mst0_ruser	WR	0x0	

STG SYSCONSAIF SYSCFG 564

Table 2-475 STG SYSCONSAIF SYSCFG 564 Register Description

Offset	0x234			
Default	0x0			
Bit	Name	Access	Default	Description
[7:0]	u1_plda_pcie_axi4_mst0_wderr	RO	0x0	
[8:31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 568

Table 2-476 STG SYSCONSAIF SYSCFG 568 Register Description

Offset	0x238			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aratomop_31_0_	WR	0x0	

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STG SYSCONSAIF SYSCFG 572

Table 2-477 STG SYSCONSAIF SYSCFG 572 Register Description

Offset	0x23c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aratomop_63_32_	WR	0x0	

STG SYSCONSAIF SYSCFG 576

Table 2-478 STG SYSCONSAIF SYSCFG 576 Register Description

Offset	0x240			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aratomop_95_64_	WR	0x0	

STG SYSCONSAIF SYSCFG 580

Table 2-479 STG SYSCONSAIF SYSCFG 580 Register Description

Offset	0x244			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aratomop_127_96_	WR	0x0	

STG SYSCONSAIF SYSCFG 584

Table 2-480 STG SYSCONSAIF SYSCFG 584 Register Description

Offset	0x248			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aratomop_159_128_	WR	0x0	

STG SYSCONSAIF SYSCFG 588

Table 2-481 STG SYSCONSAIF SYSCFG 588 Register Description

Offset	0x24c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aratomop_191_160_	WR	0x0	

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STG SYSCONSAIF SYSCFG 592

Table 2-482 STG SYSCONSAIF SYSCFG 592 Register Description

Offset	0x250			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aratomop_223_192_	WR	0x0	

STG SYSCONSAIF SYSCFG 596

Table 2-483 STG SYSCONSAIF SYSCFG 596 Register Description

Offset	0x254			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aratomop_255_224_	WR	0x0	

STG SYSCONSAIF SYSCFG 600

Table 2-484 STG SYSCONSAIF SYSCFG 600 Register Description

Offset	0x258			
Default	0x0			
Bit	Name	Access	Default	Description
[1:0]	u1_plda_pcie_axi4_slv0_aratomop_257_256_	WR	0x0	
[16:2]	u1_plda_pcie_axi4_slv0_arfunc	WR	0x0	
[20:17]	u1_plda_pcie_axi4_slv0_arregion	WR	0x0	
[31:21]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 604

Table 2-485 STG SYSCONSAIF SYSCFG 604 Register Description

Offset	0x25c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_aruser_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 608

Table 2-486 STG SYSCONSAIF SYSCFG 608 Register Description

Offset	0x260			
Default	0x0			
Bit	Name	Access	Default	Description
[8:0]	u1_plda_pcie_axi4_slv0_aruser_40_32_	WR	0x0	

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Table 2-486 STG SYSCONSAIF SYSCFG 608 Register Description (continued)

Offset	0x260			
Default	0x0			
Bit	Name	Access	Default	Description
[23:9]	u1_plda_pcie_axi4_slv0_awfunc	WR	0x0	
[27:24]	u1_plda_pcie_axi4_slv0_awregion	WR	0x0	
[31:28]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 612

Table 2-487 STG SYSCONSAIF SYSCFG 612 Register Description

Offset	0x264			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_awuser_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 616

Table 2-488 STG SYSCONSAIF SYSCFG 616 Register Description

Offset	0x268			
Default	0x0			
Bit	Name	Access	Default	Description
[8:0]	u1_plda_pcie_axi4_slv0_awuser_40_32_	WR	0x0	
[16:9]	u1_plda_pcie_axi4_slv0_rderr	RO	0x0	
[31:17]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 620

Table 2-489 STG SYSCONSAIF SYSCFG 620 Register Description

Offset	0x26c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_axi4_slv0_ruser	RO	0x0	

STG SYSCONSAIF SYSCFG 624

Table 2-490 STG SYSCONSAIF SYSCFG 624 Register Description

Offset	0x270			
Default	0x0			
Bit	Name	Access	Default	Description
[7:0]	u1_plda_pcie_axi4_slv0_wderr	WR	0x0	

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Table 2-490 STG SYSCONSAIF SYSCFG 624 Register Description (continued)

Offset	0x270			
Default	0x0			
Bit	Name	Access	Default	Description
[22:8]	u1_plda_pcie_axi4_slvl_arfunc	WR	0x0	
[31:23]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 628

Table 2-491 STG SYSCONSAIF SYSCFG 628 Register Description

Offset	0x274			
Default	0x0			
Bit	Name	Access	Default	Description
[14:0]	u1_plda_pcie_axi4_slvl_awfunc	WR	0x0	
[16:15]	u1_plda_pcie_bus_width_o	RO	0x0	
[17]	u1_plda_pcie_bypass_codec	WR	0x0	
[19:18]	u1_plda_pcie_ckref_src	WR	0x0	
[21:20]	u1_plda_pcie_clk_sel	WR	0x0	
[22]	u1_plda_pcie_clkreq	WR	0x0	
[31:23]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 632

Table 2-492 STG SYSCONSAIF SYSCFG 632 Register Description

Offset	0x278			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 636

Table 2-493 STG SYSCONSAIF SYSCFG 636 Register Description

Offset	0x27c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_63_32_	WR	0x0	

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STG SYSCONSAIF SYSCFG 640

Table 2-494 STG SYSCONSAIF SYSCFG 640 Register Description

Offset	0x280			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_95_64_	WR	0x0	

STG SYSCONSAIF SYSCFG 644

Table 2-495 STG SYSCONSAIF SYSCFG 644 Register Description

Offset	0x284			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_127_96_	WR	0x0	

STG SYSCONSAIF SYSCFG 648

Table 2-496 STG SYSCONSAIF SYSCFG 648 Register Description

Offset	0x288			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_159_128_	WR	0x0	

STG SYSCONSAIF SYSCFG 652

Table 2-497 STG SYSCONSAIF SYSCFG 652 Register Description

Offset	0x28c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_191_160_	WR	0x0	

STG SYSCONSAIF SYSCFG 656

Table 2-498 STG SYSCONSAIF SYSCFG 656 Register Description

Offset	0x290			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_223_192_	WR	0x0	

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STG SYSCONSAIF SYSCFG 660

Table 2-499 STG SYSCONSAIF SYSCFG 660 Register Description

Offset	0x294			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_255_224_	WR	0x0	

STG SYSCONSAIF SYSCFG 664

Table 2-500 STG SYSCONSAIF SYSCFG 664 Register Description

Offset	0x298			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_287_256_	WR	0x0	

STG SYSCONSAIF SYSCFG 668

Table 2-501 STG SYSCONSAIF SYSCFG 668 Register Description

Offset	0x29c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_319_288_	WR	0x0	

STG SYSCONSAIF SYSCFG 672

Table 2-502 STG SYSCONSAIF SYSCFG 672 Register Description

Offset	0x2a0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_351_320_	WR	0x0	

STG SYSCONSAIF SYSCFG 676

Table 2-503 STG SYSCONSAIF SYSCFG 676 Register Description

Offset	0x2a4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_383_352_	WR	0x0	

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STG SYSCONSAIF SYSCFG 680

Table 2-504 STG SYSCONSAIF SYSCFG 680 Register Description

Offset	0x2a8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_415_384_	WR	0x0	

STG SYSCONSAIF SYSCFG 684

Table 2-505 STG SYSCONSAIF SYSCFG 684 Register Description

Offset	0x2ac			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_447_416_	WR	0x0	

STG SYSCONSAIF SYSCFG 688

Table 2-506 STG SYSCONSAIF SYSCFG 688 Register Description

Offset	0x2b0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_479_448_	WR	0x0	

STG SYSCONSAIF SYSCFG 692

Table 2-507 STG SYSCONSAIF SYSCFG 692 Register Description

Offset	0x2b4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_511_480_	WR	0x0	

STG SYSCONSAIF SYSCFG 696

Table 2-508 STG SYSCONSAIF SYSCFG 696 Register Description

Offset	0x2b8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_543_512_	WR	0x0	

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STG SYSCONSAIF SYSCFG 700

Table 2-509 STG SYSCONSAIF SYSCFG 700 Register Description

Offset	0x2bc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_575_544_	WR	0x0	

STG SYSCONSAIF SYSCFG 704

Table 2-510 STG SYSCONSAIF SYSCFG 704 Register Description

Offset	0x2c0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_607_576_	WR	0x0	

STG SYSCONSAIF SYSCFG 708

Table 2-511 STG SYSCONSAIF SYSCFG 708 Register Description

Offset	0x2c4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_639_608_	WR	0x0	

STG SYSCONSAIF SYSCFG 712

Table 2-512 STG SYSCONSAIF SYSCFG 712 Register Description

Offset	0x2c8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_671_640_	WR	0x0	

STG SYSCONSAIF SYSCFG 716

Table 2-513 STG SYSCONSAIF SYSCFG 716 Register Description

Offset	0x2cc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_703_672_	WR	0x0	

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STG SYSCONSAIF SYSCFG 720

Table 2-514 STG SYSCONSAIF SYSCFG 720 Register Description

Offset	0x2d0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_735_704_	WR	0x0	

STG SYSCONSAIF SYSCFG 724

Table 2-515 STG SYSCONSAIF SYSCFG 724 Register Description

Offset	0x2d4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_767_736_	WR	0x0	

STG SYSCONSAIF SYSCFG 728

Table 2-516 STG SYSCONSAIF SYSCFG 728 Register Description

Offset	0x2d8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_799_768_	WR	0x0	

STG SYSCONSAIF SYSCFG 732

Table 2-517 STG SYSCONSAIF SYSCFG 732 Register Description

Offset	0x2dc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_k_phyparam_831_800_	WR	0x0	

STG SYSCONSAIF SYSCFG 736

Table 2-518 STG SYSCONSAIF SYSCFG 736 Register Description

Offset	0x2e0			
Default	0x0			
Bit	Name	Access	Default	Description
[7:0]	u1_plda_pcie_k_phyparam_839_832_	WR	0x0	
[8]	u1_plda_pcie_k_rp_nep	WR	0x0	
[9]	u1_plda_pcie_l1sub_entack	RO	0x0	
[10]	u1_plda_pcie_l1sub_entreq	WR	0x0	

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Table 2-518 STG SYSCONSAIF SYSCFG 736 Register Description (continued)

Offset	0x2e0			
Default	0x0			
Bit	Name	Access	Default	Description
[31:11]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 740

Table 2-519 STG SYSCONSAIF SYSCFG 740 Register Description

Offset	0x2e4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_local_interrupt_in	WR	0x0	

STG SYSCONSAIF SYSCFG 744

Table 2-520 STG SYSCONSAIF SYSCFG 744 Register Description

Offset	0x2e8			
Default	0x4800001			
Bit	Name	Access	Default	Description
[0]	u1_plda_pcie_mperstn	WR	0x1	
[1]	u1_plda_pcie_pcie_ebuf_mode	WR	0x0	
[24:2]	u1_plda_pcie_pcie_phy_test_cfg	WR	0x200000	
[25]	u1_plda_pcie_pcie_rx_eq_training	WR	0x0	
[26]	u1_plda_pcie_pcie_rxterm_en	WR	0x1	
[27]	u1_plda_pcie_pcie_tx_oneszeros	WR	0x0	
[31:28]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 748

Table 2-521 STG SYSCONSAIF SYSCFG 748 Register Description

Offset	0x2ec			
Default	0x0			
Bit	Name	Access	Default	Description
[19:0]	u1_plda_pcie_pf0_offset	WR	0x0	
[31:20]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 752

Table 2-522 STG SYSCONSAIF SYSCFG 752 Register Description

Offset	0x2f0			
Default	0x0			
Bit	Name	Access	Default	Description
[19:0]	u1_plda_pcie_pf1_offset	WR	0x0	
[31:20]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 756

Table 2-523 STG SYSCONSAIF SYSCFG 756 Register Description

Offset	0x2f4			
Default	0x0			
Bit	Name	Access	Default	Description
[19:0]	u1_plda_pcie_pf2_offset	WR	0x0	
[31:20]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 760

Table 2-524 STG SYSCONSAIF SYSCFG 760 Register Description

Offset	0x2f8			
Default	0x0			
Bit	Name	Access	Default	Description
[19:0]	u1_plda_pcie_pf3_offset	WR	0x0	
[21:20]	u1_plda_pcie_phy_mode	WR	0x0	
[22]	u1_plda_pcie_pl_clkrem_allow	WR	0x0	
[23]	u1_plda_pcie_pl_clkreq_oen	RO	0x0	
[25:24]	u1_plda_pcie_pl_equ_phase	RO	0x0	
[30:26]	u1_plda_pcie_pl_ltssm	RO	0x0	
[31]	Reserved	None	0x0	Reserved

STG SYSCONSAIF SYSCFG 764

Table 2-525 STG SYSCONSAIF SYSCFG 764 Register Description

Offset	0x2fc			
Default	0x0			
Bit	Name	Access	Default	Description
[4:0]	u1_plda_pcie_pl_pclk_rate	RO	0x0	
[31:5]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 768

Table 2-526 STG SYSCONSAIF SYSCFG 768 Register Description

Offset	0x300			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_pl_sideband_in_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 772

Table 2-527 STG SYSCONSAIF SYSCFG 772 Register Description

Offset	0x304			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_pl_sideband_in_63_32_	WR	0x0	

STG SYSCONSAIF SYSCFG 776

Table 2-528 STG SYSCONSAIF SYSCFG 776 Register Description

Offset	0x308			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_pl_sideband_out_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 780

Table 2-529 STG SYSCONSAIF SYSCFG 780 Register Description

Offset	0x30c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_pl_sideband_out_63_32_	RO	0x0	

STG SYSCONSAIF SYSCFG 784

Table 2-530 STG SYSCONSAIF SYSCFG 784 Register Description

Offset	0x310			
Default	0x1			
Bit	Name	Access	Default	Description
[0]	u1_plda_pcie_pl_wake_in	WR	0x1	
[1]	u1_plda_pcie_pl_wake_oen	RO	0x0	
[2]	u1_plda_pcie_rx_standby_o	RO	0x0	
[31:3]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 788

Table 2-531 STG SYSCONSAIF SYSCFG 788 Register Description

Offset	0x314			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_in_31_0_	WR	0x0	

STG SYSCONSAIF SYSCFG 792

Table 2-532 STG SYSCONSAIF SYSCFG 792 Register Description

Offset	0x318			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_in_63_32_	WR	0x0	

STG SYSCONSAIF SYSCFG 796

Table 2-533 STG SYSCONSAIF SYSCFG 796 Register Description

Offset	0x31c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 800

Table 2-534 STG SYSCONSAIF SYSCFG 800 Register Description

Offset	0x320			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_63_32_	RO	0x0	

STG SYSCONSAIF SYSCFG 804

Table 2-535 STG SYSCONSAIF SYSCFG 804 Register Description

Offset	0x324			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_95_64_	RO	0x0	

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STG SYSCONSAIF SYSCFG 808

Table 2-536 STG SYSCONSAIF SYSCFG 808 Register Description

Offset	0x328			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_127_96_	RO	0x0	

STG SYSCONSAIF SYSCFG 812

Table 2-537 STG SYSCONSAIF SYSCFG 812 Register Description

Offset	0x32c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_159_128_	RO	0x0	

STG SYSCONSAIF SYSCFG 816

Table 2-538 STG SYSCONSAIF SYSCFG 816 Register Description

Offset	0x330			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_191_160_	RO	0x0	

STG SYSCONSAIF SYSCFG 820

Table 2-539 STG SYSCONSAIF SYSCFG 820 Register Description

Offset	0x334			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_223_192_	RO	0x0	

STG SYSCONSAIF SYSCFG 824

Table 2-540 STG SYSCONSAIF SYSCFG 824 Register Description

Offset	0x338			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_255_224_	RO	0x0	

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STG SYSCONSAIF SYSCFG 828

Table 2-541 STG SYSCONSAIF SYSCFG 828 Register Description

Offset	0x33c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_287_256_	RO	0x0	

STG SYSCONSAIF SYSCFG 832

Table 2-542 STG SYSCONSAIF SYSCFG 832 Register Description

Offset	0x340			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_319_288_	RO	0x0	

STG SYSCONSAIF SYSCFG 836

Table 2-543 STG SYSCONSAIF SYSCFG 836 Register Description

Offset	0x344			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_351_320_	RO	0x0	

STG SYSCONSAIF SYSCFG 840

Table 2-544 STG SYSCONSAIF SYSCFG 840 Register Description

Offset	0x348			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_383_352_	RO	0x0	

STG SYSCONSAIF SYSCFG 844

Table 2-545 STG SYSCONSAIF SYSCFG 844 Register Description

Offset	0x34c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_415_384_	RO	0x0	

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STG SYSCONSAIF SYSCFG 848

Table 2-546 STG SYSCONSAIF SYSCFG 848 Register Description

Offset	0x350			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_447_416_	RO	0x0	

STG SYSCONSAIF SYSCFG 852

Table 2-547 STG SYSCONSAIF SYSCFG 852 Register Description

Offset	0x354			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_479_448_	RO	0x0	

STG SYSCONSAIF SYSCFG 856

Table 2-548 STG SYSCONSAIF SYSCFG 856 Register Description

Offset	0x358			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_bridge_511_480_	RO	0x0	

STG SYSCONSAIF SYSCFG 860

Table 2-549 STG SYSCONSAIF SYSCFG 860 Register Description

Offset	0x35c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_31_0_	RO	0x0	

STG SYSCONSAIF SYSCFG 864

Table 2-550 STG SYSCONSAIF SYSCFG 864 Register Description

Offset	0x360			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_63_32_	RO	0x0	

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STG SYSCONSAIF SYSCFG 868

Table 2-551 STG SYSCONSAIF SYSCFG 868 Register Description

Offset	0x364			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_95_64_	RO	0x0	

STG SYSCONSAIF SYSCFG 872

Table 2-552 STG SYSCONSAIF SYSCFG 872 Register Description

Offset	0x368			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_127_96_	RO	0x0	

STG SYSCONSAIF SYSCFG 876

Table 2-553 STG SYSCONSAIF SYSCFG 876 Register Description

Offset	0x36c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_159_128_	RO	0x0	

STG SYSCONSAIF SYSCFG 880

Table 2-554 STG SYSCONSAIF SYSCFG 880 Register Description

Offset	0x370			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_191_160_	RO	0x0	

STG SYSCONSAIF SYSCFG 884

Table 2-555 STG SYSCONSAIF SYSCFG 884 Register Description

Offset	0x374			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_223_192_	RO	0x0	

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STG SYSCONSAIF SYSCFG 888

Table 2-556 STG SYSCONSAIF SYSCFG 888 Register Description

Offset	0x378			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_255_224_	RO	0x0	

STG SYSCONSAIF SYSCFG 892

Table 2-557 STG SYSCONSAIF SYSCFG 892 Register Description

Offset	0x37c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_287_256_	RO	0x0	

STG SYSCONSAIF SYSCFG 896

Table 2-558 STG SYSCONSAIF SYSCFG 896 Register Description

Offset	0x380			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_319_288_	RO	0x0	

STG SYSCONSAIF SYSCFG 900

Table 2-559 STG SYSCONSAIF SYSCFG 900 Register Description

Offset	0x384			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_351_320_	RO	0x0	

STG SYSCONSAIF SYSCFG 904

Table 2-560 STG SYSCONSAIF SYSCFG 904 Register Description

Offset	0x388			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_383_352_	RO	0x0	

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STG SYSCONSAIF SYSCFG 908

Table 2-561 STG SYSCONSAIF SYSCFG 908 Register Description

Offset	0x38c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_415_384_	RO	0x0	

STG SYSCONSAIF SYSCFG 912

Table 2-562 STG SYSCONSAIF SYSCFG 912 Register Description

Offset	0x390			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_447_416_	RO	0x0	

STG SYSCONSAIF SYSCFG 916

Table 2-563 STG SYSCONSAIF SYSCFG 916 Register Description

Offset	0x394			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_479_448_	RO	0x0	

STG SYSCONSAIF SYSCFG 920

Table 2-564 STG SYSCONSAIF SYSCFG 920 Register Description

Offset	0x398			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u1_plda_pcie_test_out_pcie_511_480_	RO	0x0	

STG SYSCONSAIF SYSCFG 924

Table 2-565 STG SYSCONSAIF SYSCFG 924 Register Description

Offset	0x39c			
Default	0xc80			
Bit	Name	Access	Default	Description
[0:3]	u1_plda_pcie_test_sel	WR	0x0	
[25:4]	u1_plda_pcie_tl_clock_freq	WR	0xc8	
[31:26]	Reserved	None	0x0	Reserved

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STG SYSCONSAIF SYSCFG 928

Table 2-566 STG SYSCONSAIF SYSCFG 928 Register Description

Offset	0x3a0			
Default	0x0			
Bit	Name	Access	Default	Description
[15:0]	u1_plda_pcie_tl_ctrl_hotplug	RO	0x0	
[31:16]	u1_plda_pcie_tl_report_hotplug	WR	0x0	

STG SYSCONSAIF SYSCFG 932

Table 2-567 STG SYSCONSAIF SYSCFG 932 Register Description

Offset	0x3a4			
Default	0x8			
Bit	Name	Access	Default	Description
[1:0]	u1_plda_pcie_tx_pattern	WR	0x0	
[2:3]	u1_plda_pcie_usb3_bus_width	WR	0x2	
[4]	u1_plda_pcie_usb3_phy_enable	WR	0x0	
[6:5]	u1_plda_pcie_usb3_rate	WR	0x0	
[7]	u1_plda_pcie_usb3_rx_standby	WR	0x0	
[8]	u1_plda_pcie_xwdecerr	RO	0x0	
[9]	u1_plda_pcie_xwerrclr	WR	0x0	
[10]	u1_plda_pcie_xwslverr	RO	0x0	
[31:11]	Reserved	None	0x0	Reserved

2.8.6. AON SYSCON

The JH-7110 system provides the following AON SYSCON Always-ON (AON) control registers which provides clock and reset signals to interfaces with master and/or slave signals.

AON SYSCONSAIF SYSCFG 0

Table 2-568 AON SYSCONSAIF SYSCFG 0 Register Description

Offset	0x0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	aon_gp_reg	WR	0x0	

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AON SYSCONSAIF SYSCFG 4

Table 2-569 AON SYSCONSAIF SYSCFG 4 Register Description

Offset	0x4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	u0_boot_ctrl_boot_status	RO	0x0	
[4:31]	Reserved	None	0x0	Reserved

AON SYSCONSAIF SYSCFG 8

Table 2-570 AON SYSCONSAIF SYSCFG 8 Register Description

Offset	0x8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_boot_ctrl_boot_vector_31_0_	RO	0x0	

AON SYSCONSAIF SYSCFG 12

Table 2-571 AON SYSCONSAIF SYSCFG 12 Register Description

Offset	0xc			
Default	0x4d540			
Bit	Name	Access	Default	Description
[0:3]	u0_boot_ctrl_boot_vector_35_32_	RO	0x0	
[15:4]	gmac5_axi64_SCFG_ram_cfg	WR	0xd54	SRAM/ROM configuration. • [4]: SLP, sleep enable, high active, default is low. • [5]: SD, shutdown enable, high active, default is low. • [6:7]: RTSEL, timing setting for debug purpose, default is 2'b01 • [8:9]: PTSEL, timing setting for debug purpose, default is 2'b01 • [11:10]: TRB, timing setting for debug purpose, default is 2'b01 • [13:12]: WTSEL, timing setting for debug purpose, default is 2'b01 • [14]: VS, timing setting for debug purpose, default is 1'b1 • [15]: VG, timing setting for debug purpose, default is 1'b1

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Table 2-571 AON SYSCONSAIF SYSCFG 12 Register Description (continued)

Offset	0xc			
Default	0x4d540			
Bit	Name	Access	Default	Description
[17:16]	gmac5_axi64_mac_-speed_o	RO	0x0	
[20:18]	gmac5_axi64_phy_intf_-sel_i	WR	0x1	Active PHY Selected When you have multiple GMAC PHY interfaces in your configuration, this field indicates the sampled value of the PHY selector during reset de-assertion. Values: • 0x0(GMII_MII): GMII or MII • 0x1(RGMII): RGMII • 0x2(SGMII): SGMII • 0x3(TBI): TBI • 0x4(RMII): RMII • 0x5(RTBI): RTBI • 0x6(SMII): SMII • 0x7(REVMIII): RevMII
[31:21]	Reserved	None	0x0	Reserved

AON SYSCONSAIF SYSCFG 16

Table 2-572 AON SYSCONSAIF SYSCFG 16 Register Description

Offset	0x10			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	gmac5_axi64_ptp_timestamp_o_31_-0_	RO	0x0	

AON SYSCONSAIF SYSCFG 20

Table 2-573 AON SYSCONSAIF SYSCFG 20 Register Description

Offset	0x14			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	gmac5_axi64_ptp_timestamp_o_63_-32_	RO	0x0	

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AON SYSCONSAIF SYSCFG 24

Table 2-574 AON SYSCONSAIF SYSCFG 24 Register Description

Offset	0x18			
Default	0x0			
Bit	Name	Access	Default	Description
[0]	u0_otpc_chip_mode	RO	0x0	
[1]	u0_otpc_crc_pass	RO	0x0	
[2]	u0_otpc_dbg_enable	RO	0x0	
[31:3]	Reserved	None	0x0	Reserved

AON SYSCONSAIF SYSCFG 28

Table 2-575 AON SYSCONSAIF SYSCFG 28 Register Description

Offset	0x1c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_otpc_fl_func_lock	RO	0x0	

AON SYSCONSAIF SYSCFG 32

Table 2-576 AON SYSCONSAIF SYSCFG 32 Register Description

Offset	0x20			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_otpc_fl_pll0_lock	RO	0x0	

AON SYSCONSAIF SYSCFG 36

Table 2-577 AON SYSCONSAIF SYSCFG 36 Register Description

Offset	0x24			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	u0_otpc_fl_pll1_lock	RO	0x0	

AON SYSCONSAIF SYSCFG 40

Table 2-578 AON SYSCONSAIF SYSCFG 40 Register Description

Offset	0x28			
Default	0x20			
Bit	Name	Access	Default	Description
[0]	u0_otpc_fl_sec_boot_lmt	RO	0x0	

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Table 2-578 AON SYSCONSAIF SYSCFG 40 Register Description (continued)

Offset	0x28			
Default	**0x20**			
Bit	**Name**	**Access**	**Default**	**Description**
[1]	u0_otpc_fl_xip	RO	0x0	
[2]	u0_otpc_load_busy	RO	0x0	
[3]	u0_reset_ctrl_clr_reset_status	WR	0x0	
[4]	u0_reset_ctrl_pll_timecnt_finish	RO	0x0	
[5]	u0_reset_ctrl_rstn_sw	WR	0x1	
[9:6]	u0_reset_ctrl_sys_reset_status	RO	0x0	
[10:31]	Reserved	None	0x0	Reserved

2.8.7. SYS IOMUX CFG

The JH-7110 system provides the following SYS IOMUX CFG registers for system IO multiplexing configuration.

SYS IOMUX CFGSAIF SYSCFG FMUX 0

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO0 - GPIO3.

Table 2-579 SYS IOMUX CFGSAIF SYSCFG FMUX 0 Register Description

Offset	0x0			
Default	**0x8010101**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo0_doen_cfg	WR	0x1	The selected OEN signal for GPIO0. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo1_doen_cfg	WR	0x1	The selected OEN signal for GPIO1. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo2_doen_cfg	WR	0x1	The selected OEN signal for GPIO2. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved

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Table 2-579 SYS IOMUX CFGSAIF SYSCFG FMUX 0 Register Description (continued)

Offset	0x0			
Default	**0x8010101**			
Bit	**Name**	**Access**	**Default**	**Description**
[24:29]	sys_iomux_gpo3_doen_cfg	WR	0x8	The selected OEN signal for GPIO3. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 1

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO4 - GPIO7.

Table 2-580 SYS IOMUX CFGSAIF SYSCFG FMUX 1 Register Description

Offset	0x4			
Default	**0x10001**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo4_doen_cfg	WR	0x1	The selected OEN signal for GPIO4. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo5_doen_cfg	WR	0x0	The selected OEN signal for GPIO5. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo6_doen_cfg	WR	0x1	The selected OEN signal for GPIO6. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo7_doen_cfg	WR	0x0	The selected OEN signal for GPIO7. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFGSAIF SYSCFG FMUX 2

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO8 - GPIO11.

Table 2-581 SYS IOMUX CFGSAIF SYSCFG FMUX 2 Register Description

Offset	0x8			
Default	0x7010100			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo8_doen_cfg	WR	0x0	The selected OEN signal for GPIO8. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo9_doen_cfg	WR	0x1	The selected OEN signal for GPIO9. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo10_doen_cfg	WR	0x1	The selected OEN signal for GPIO10. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo11_doen_cfg	WR	0x7	The selected OEN signal for GPIO11. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 3

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO12 - GPIO15.

Table 2-582 SYS IOMUX CFGSAIF SYSCFG FMUX 3 Register Description

Offset	0xc			
Default	0x101			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo12_doen_cfg	WR	0x1	The selected OEN signal for GPIO12. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list

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Table 2-582 SYS IOMUX CFGSAIF SYSCFG FMUX 3 Register Description (continued)

Offset	0xc			
Default	**0x101**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo13_doen_cfg	WR	0x1	The selected OEN signal for GPIO13. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo14_doen_cfg	WR	0x0	The selected OEN signal for GPIO14. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo15_doen_cfg	WR	0x0	The selected OEN signal for GPIO15. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 4

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO16 - GPIO19.

Table 2-583 SYS IOMUX CFGSAIF SYSCFG FMUX 4 Register Description

Offset	0x10			
Default	**0x1000000**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo16_doen_cfg	WR	0x0	The selected OEN signal for GPIO16. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo17_doen_cfg	WR	0x0	The selected OEN signal for GPIO17. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list

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Table 2-583 SYS IOMUX CFGSAIF SYSCFG FMUX 4 Register Description (continued)

Offset	0x10			
Default	**0x1000000**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo18_doen_cfg	WR	0x0	The selected OEN signal for GPIO18. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo19_doen_cfg	WR	0x1	The selected OEN signal for GPIO19. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 5

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO20 - GPIO23.

Table 2-584 SYS IOMUX CFGSAIF SYSCFG FMUX 5 Register Description

Offset	0x14			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo20_doen_cfg	WR	0x0	The selected OEN signal for GPIO20. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo21_doen_cfg	WR	0x0	The selected OEN signal for GPIO21. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo22_doen_cfg	WR	0x0	The selected OEN signal for GPIO22. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list

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Table 2-584 SYS IOMUX CFGSAIF SYSCFG FMUX 5 Register Description (continued)

Offset	0x14			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo23_doen_cfg	WR	0x0	The selected OEN signal for GPIO23. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 6

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO24 - GPIO27.

Table 2-585 SYS IOMUX CFGSAIF SYSCFG FMUX 6 Register Description

Offset	0x18			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo24_doen_cfg	WR	0x0	The selected OEN signal for GPIO24. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo25_doen_cfg	WR	0x0	The selected OEN signal for GPIO25. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo26_doen_cfg	WR	0x0	The selected OEN signal for GPIO26. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo27_doen_cfg	WR	0x0	The selected OEN signal for GPIO27. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list

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Table 2-585 SYS IOMUX CFGSAIF SYSCFG FMUX 6 Register Description (continued)

Offset	0x18			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 7

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO28 - GPIO31.

Table 2-586 SYS IOMUX CFGSAIF SYSCFG FMUX 7 Register Description

Offset	0x1c			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo28_doen_cfg	WR	0x0	The selected OEN signal for GPIO28. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo29_doen_cfg	WR	0x0	The selected OEN signal for GPIO29. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo30_doen_cfg	WR	0x0	The selected OEN signal for GPIO30. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo31_doen_cfg	WR	0x0	The selected OEN signal for GPIO31. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 8

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO32 - GPIO35.

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Table 2-587 SYS IOMUX CFGSAIF SYSCFG FMUX 8 Register Description

Offset	0x20			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo32_doen_cfg	WR	0x0	The selected OEN signal for GPIO32. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo33_doen_cfg	WR	0x0	The selected OEN signal for GPIO33. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo34_doen_cfg	WR	0x0	The selected OEN signal for GPIO34. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo35_doen_cfg	WR	0x0	The selected OEN signal for GPIO35. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 9

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO36 - GPIO39.

Table 2-588 SYS IOMUX CFGSAIF SYSCFG FMUX 9 Register Description

Offset	0x24			
Default	**0x23220605**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo36_doen_cfg	WR	0x5	The selected OEN signal for GPIO36. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved

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Table 2-588 SYS IOMUX CFGSAIF SYSCFG FMUX 9 Register Description (continued)

Offset	0x24			
Default	0x23220605			
Bit	Name	Access	Default	Description
[13:8]	sys_iomux_gpo37_doen_cfg	WR	0x6	The selected OEN signal for GPIO37. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo38_doen_cfg	WR	0x22	The selected OEN signal for GPIO38. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo39_doen_cfg	WR	0x23	The selected OEN signal for GPIO39. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 10

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO40 - GPIO43.

Table 2-589 SYS IOMUX CFGSAIF SYSCFG FMUX 10 Register Description

Offset	0x28			
Default	0x1000001			
Bit	Name	Access	Default	Description
[5:0]	sys_iomux_gpo40_doen_cfg	WR	0x1	The selected OEN signal for GPIO40. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo41_doen_cfg	WR	0x0	The selected OEN signal for GPIO41. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved

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Table 2-589 SYS IOMUX CFGSAIF SYSCFG FMUX 10 Register Description (continued)

Offset	0x28			
Default	**0x1000001**			
Bit	**Name**	**Access**	**Default**	**Description**
[21:16]	sys_iomux_gpo42_doen_cfg	WR	0x0	The selected OEN signal for GPIO42. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo43_doen_cfg	WR	0x1	The selected OEN signal for GPIO43. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 11

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO44 - GPIO47.

Table 2-590 SYS IOMUX CFGSAIF SYSCFG FMUX 11 Register Description

Offset	0x2c			
Default	**0x1000001**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo44_doen_cfg	WR	0x1	The selected OEN signal for GPIO44. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo45_doen_cfg	WR	0x0	The selected OEN signal for GPIO45. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo46_doen_cfg	WR	0x0	The selected OEN signal for GPIO46. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved

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Table 2-590 SYS IOMUX CFGSAIF SYSCFG FMUX 11 Register Description (continued)

Offset	0x2c			
Default	0x1000001			
Bit	Name	Access	Default	Description
[24:29]	sys_iomux_gpo47_doen_cfg	WR	0x1	The selected OEN signal for GPIO47. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 12

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO48 - GPIO51.

Table 2-591 SYS IOMUX CFGSAIF SYSCFG FMUX 12 Register Description

Offset	0x30			
Default	0xe010d0d			
Bit	Name	Access	Default	Description
[5:0]	sys_iomux_gpo48_doen_cfg	WR	0xd	The selected OEN signal for GPIO48. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo49_doen_cfg	WR	0xd	The selected OEN signal for GPIO49. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo50_doen_cfg	WR	0x1	The selected OEN signal for GPIO50. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo51_doen_cfg	WR	0xe	The selected OEN signal for GPIO51. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFGSAIF SYSCFG FMUX 13

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO52 - GPIO55.

Table 2-592 SYS IOMUX CFGSAIF SYSCFG FMUX 13 Register Description

Offset	0x34			
Default	0x1d011c1c			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo52_doen_cfg	WR	0x1c	The selected OEN signal for GPIO52. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo53_doen_cfg	WR	0x1c	The selected OEN signal for GPIO53. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo54_doen_cfg	WR	0x1	The selected OEN signal for GPIO54. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo55_doen_cfg	WR	0x1d	The selected OEN signal for GPIO55. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 14

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO56 - GPIO59.

Table 2-593 SYS IOMUX CFGSAIF SYSCFG FMUX 14 Register Description

Offset	0x38			
Default	0x25012424			
Bit	**Name**	**Access**	**Default**	**Description**
5:0]	sys_iomux_gpo56_doen_cfg	WR	0x24	The selected OEN signal for GPIO56. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list

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Table 2-593 SYS IOMUX CFGSAIF SYSCFG FMUX 14 Register Description (continued)

Offset	0x38			
Default	**0x25012424**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo57_doen_cfg	WR	0x24	The selected OEN signal for GPIO57. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo58_doen_cfg	WR	0x1	The selected OEN signal for GPIO58. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo59_doen_cfg	WR	0x25	The selected OEN signal for GPIO59. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 15

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO60 - GPIO63.

Table 2-594 SYS IOMUX CFGSAIF SYSCFG FMUX 15 Register Description

Offset	0x3c			
Default	**0x29012828**			
Bit	**Name**	**Access**	**Default**	**Description**
[5:0]	sys_iomux_gpo60_doen_cfg	WR	0x28	The selected OEN signal for GPIO60. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[6:7]	Reserved	None	0x0	Reserved
[13:8]	sys_iomux_gpo61_doen_cfg	WR	0x28	The selected OEN signal for GPIO61. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list

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Table 2-594 SYS IOMUX CFGSAIF SYSCFG FMUX 15 Register Description (continued)

Offset	0x3c			
Default	**0x29012828**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15:14]	Reserved	None	0x0	Reserved
[21:16]	sys_iomux_gpo62_doen_cfg	WR	0x1	The selected OEN signal for GPIO62. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23:22]	Reserved	None	0x0	Reserved
[24:29]	sys_iomux_gpo63_doen_cfg	WR	0x29	The selected OEN signal for GPIO63. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-49. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 16

The register can be used to configure the selected output signal for GPIO0 - GPIO3.

Table 2-595 SYS IOMUX CFGSAIF SYSCFG FMUX 16 Register Description

Offset	0x40			
Default	**0x16000000**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo0_dout_cfg	WR	0x0	The selected output signal for GPIO0. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo1_dout_cfg	WR	0x0	The selected output signal for GPIO1. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo2_dout_cfg	WR	0x0	The selected output signal for GPIO2. The register value indicates the selected GPIO output signal index from GPIO output signal list

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Table 2-595 SYS IOMUX CFGSAIF SYSCFG FMUX 16 Register Description (continued)

Offset	0x40			
Default	0x16000000			
Bit	Name	Access	Default	Description
				0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo3_dout_cfg	WR	0x16	The selected output signal for GPIO3. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 17

The register can be used to configure the selected output signal for GPIO4 - GPIO7.

Table 2-596 SYS IOMUX CFGSAIF SYSCFG FMUX 17 Register Description

Offset	0x44			
Default	0x1400			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpo4_dout_cfg	WR	0x0	The selected output signal for GPIO4. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo5_dout_cfg	WR	0x14	The selected output signal for GPIO5. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo6_dout_cfg	WR	0x0	The selected output signal for GPIO6. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo7_dout_cfg	WR	0x0	The selected output signal for GPIO7. The register value indicates the selected GPIO output signal index from GPIO output signal list

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Table 2-596 SYS IOMUX CFGSAIF SYSCFG FMUX 17 Register Description (continued)

Offset	0x44			
Default	0x1400			
Bit	Name	Access	Default	Description
				0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 18

The register can be used to configure the selected output signal for GPIO8 - GPIO11.

Table 2-597 SYS IOMUX CFGSAIF SYSCFG FMUX 18 Register Description

Offset	0x48			
Default	0x15000000			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpo8_dout_cfg	WR	0x0	The selected output signal for GPIO8. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo9_dout_cfg	WR	0x0	The selected output signal for GPIO9. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo10_dout_cfg	WR	0x0	The selected output signal for GPIO10. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo11_dout_cfg	WR	0x15	The selected output signal for GPIO11. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 19

The register can be used to configure the selected output signal for GPIO12 - GPIO15.

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Table 2-598 SYS IOMUX CFGSAIF SYSCFG FMUX 19 Register Description

Offset	0x4c			
Default	0x0			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpo12_dout_cfg	WR	0x0	The selected output signal for GPIO12. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo13_dout_cfg	WR	0x0	The selected output signal for GPIO13. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo14_dout_cfg	WR	0x0	The selected output signal for GPIO14. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo15_dout_cfg	WR	0x0	The selected output signal for GPIO15. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 20

The register can be used to configure the selected output signal for GPIO16 - GPIO19.

Table 2-599 SYS IOMUX CFGSAIF SYSCFG FMUX 20 Register Description

Offset	0x50			
Default	0x550000			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpo16_dout_cfg	WR	0x0	The selected output signal for GPIO16. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved

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Table 2-599 SYS IOMUX CFGSAIF SYSCFG FMUX 20 Register Description (continued)

Offset	0x50			
Default	**0x550000**			
Bit	**Name**	**Access**	**Default**	**Description**
[14:8]	sys_iomux_gpo17_dout_cfg	WR	0x0	The selected output signal for GPIO17. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo18_dout_cfg	WR	0x55	The selected output signal for GPIO18. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo19_dout_cfg	WR	0x0	The selected output signal for GPIO19. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 21

The register can be used to configure the selected output signal for GPIO20 - GPIO23.

Table 2-600 SYS IOMUX CFGSAIF SYSCFG FMUX 21 Register Description

Offset	0x54			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo20_dout_cfg	WR	0x0	The selected output signal for GPIO20. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo21_dout_cfg	WR	0x0	The selected output signal for GPIO21. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved

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Table 2-600 SYS IOMUX CFGSAIF SYSCFG FMUX 21 Register Description (continued)

Offset	0x54			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[22:16]	sys_iomux_gpo22_dout_cfg	WR	0x0	The selected output signal for GPIO22. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo23_dout_cfg	WR	0x0	The selected output signal for GPIO23. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 22

The register can be used to configure the selected output signal for GPIO24 - GPIO27.

Table 2-601 SYS IOMUX CFGSAIF SYSCFG FMUX 22 Register Description

Offset	0x58			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo24_dout_cfg	WR	0x0	The selected output signal for GPIO24. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo25_dout_cfg	WR	0x0	The selected output signal for GPIO25. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo26_dout_cfg	WR	0x0	The selected output signal for GPIO26. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved

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Table 2-601 SYS IOMUX CFGSAIF SYSCFG FMUX 22 Register Description (continued)

Offset	0x58			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[30:24]	sys_iomux_gpo27_dout_cfg	WR	0x0	The selected output signal for GPIO27. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 23

The register can be used to configure the selected output signal for GPIO28 - GPIO31.

Table 2-602 SYS IOMUX CFGSAIF SYSCFG FMUX 23 Register Description

Offset	0x5c			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo28_dout_cfg	WR	0x0	The selected output signal for GPIO28. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo29_dout_cfg	WR	0x0	The selected output signal for GPIO29. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo30_dout_cfg	WR	0x0	The selected output signal for GPIO30. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo31_dout_cfg	WR	0x0	The selected output signal for GPIO31. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFGSAIF SYSCFG FMUX 24

The register can be used to configure the selected output signal for GPIO32 - GPIO35.

Table 2-603 SYS IOMUX CFGSAIF SYSCFG FMUX 24 Register Description

Offset	0x60			
Default	0xd000000			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo32_dout_cfg	WR	0x0	The selected output signal for GPIO32. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo33_dout_cfg	WR	0x0	The selected output signal for GPIO33. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo34_dout_cfg	WR	0x0	The selected output signal for GPIO34. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo35_dout_cfg	WR	0xd	The selected output signal for GPIO35. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 25

The register can be used to configure the selected output signal for GPIO36 - GPIO39.

Table 2-604 SYS IOMUX CFGSAIF SYSCFG FMUX 25 Register Description

Offset	0x64			
Default	0x54530f0e			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo36_dout_cfg	WR	0xe	The selected output signal for GPIO36. The register value indicates the selected GPIO output signal index from GPIO output signal list

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Table 2-604 SYS IOMUX CFGSAIF SYSCFG FMUX 25 Register Description (continued)

Offset	0x64			
Default	**0x54530f0e**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo37_dout_cfg	WR	0xf	The selected output signal for GPIO37. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo38_dout_cfg	WR	0x53	The selected output signal for GPIO38. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo39_dout_cfg	WR	0x54	The selected output signal for GPIO39. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 26

The register can be used to configure the selected output signal for GPIO40 - GPIO43.

Table 2-605 SYS IOMUX CFGSAIF SYSCFG FMUX 26 Register Description

Offset	0x68			
Default	**0x4e4f00**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo40_dout_cfg	WR	0x0	The selected output signal for GPIO40. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo41_dout_cfg	WR	0x4f	The selected output signal for GPIO41. The register value indicates the selected GPIO output signal index from GPIO output signal list

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Table 2-605 SYS IOMUX CFGSAIF SYSCFG FMUX 26 Register Description (continued)

Offset	0x68			
Default	**0x4e4f00**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo42_dout_cfg	WR	0x4e	The selected output signal for GPIO42. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo43_dout_cfg	WR	0x0	The selected output signal for GPIO43. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 27

The register can be used to configure the selected output signal for GPIO44 - GPIO47.

Table 2-606 SYS IOMUX CFGSAIF SYSCFG FMUX 27 Register Description

Offset	0x6c			
Default	**0x5b5c00**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo44_dout_cfg	WR	0x0	The selected output signal for GPIO44. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo45_dout_cfg	WR	0x5c	The selected output signal for GPIO45. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo46_dout_cfg	WR	0x5b	The selected output signal for GPIO46. The register value indicates the selected GPIO output signal index from GPIO output signal list

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Table 2-606 SYS IOMUX CFGSAIF SYSCFG FMUX 27 Register Description (continued)

Offset	0x6c			
Default	**0x5b5c00**			
Bit	**Name**	**Access**	**Default**	**Description**
				0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo47_dout_cfg	WR	0x0	The selected output signal for GPIO47. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 28

The register can be used to configure the selected output signal for GPIO48 - GPIO51.

Table 2-607 SYS IOMUX CFGSAIF SYSCFG FMUX 28 Register Description

Offset	0x70			
Default	**0x20001e1f**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpo48_dout_cfg	WR	0x1f	The selected output signal for GPIO48. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo49_dout_cfg	WR	0x1e	The selected output signal for GPIO49. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo50_dout_cfg	WR	0x0	The selected output signal for GPIO50. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo51_dout_cfg	WR	0x20	The selected output signal for GPIO51. The register value indicates the selected GPIO output signal index from GPIO output signal list

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Table 2-607 SYS IOMUX CFGSAIF SYSCFG FMUX 28 Register Description (continued)

Offset	0x70			
Default	0x20001e1f			
Bit	Name	Access	Default	Description
				0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 29

The register can be used to configure the selected output signal for GPIO52 - GPIO55.

Table 2-608 SYS IOMUX CFGSAIF SYSCFG FMUX 29 Register Description

Offset	0x74			
Default	0x4b00494a			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpo52_dout_cfg	WR	0x4a	The selected output signal for GPIO52. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo53_dout_cfg	WR	0x49	The selected output signal for GPIO53. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo54_dout_cfg	WR	0x0	The selected output signal for GPIO54. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo55_dout_cfg	WR	0x4b	The selected output signal for GPIO55. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 30

The register can be used to configure the selected output signal for GPIO56 - GPIO59.

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Table 2-609 SYS IOMUX CFGSAIF SYSCFG FMUX 30 Register Description

Offset	0x78			
Default	0x58005657			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpo56_dout_cfg	WR	0x57	The selected output signal for GPIO56. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpo57_dout_cfg	WR	0x56	The selected output signal for GPIO57. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo58_dout_cfg	WR	0x0	The selected output signal for GPIO58. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo59_dout_cfg	WR	0x58	The selected output signal for GPIO59. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 31

The register can be used to configure the selected output signal for GPIO60 - GPIO63.

Table 2-610 SYS IOMUX CFGSAIF SYSCFG FMUX 31 Register Description

Offset	0x7c			
Default	0x5f005d5e			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpo60_dout_cfg	WR	0x5e	The selected output signal for GPIO60. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[7]	Reserved	None	0x0	Reserved

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Table 2-610 SYS IOMUX CFGSAIF SYSCFG FMUX 31 Register Description (continued)

Offset	0x7c			
Default	**0x5f005d5e**			
Bit	**Name**	**Access**	**Default**	**Description**
[14:8]	sys_iomux_gpo61_dout_cfg	WR	0x5d	The selected output signal for GPIO61. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpo62_dout_cfg	WR	0x0	The selected output signal for GPIO62. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpo63_dout_cfg	WR	0x5f	The selected output signal for GPIO63. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-107. See Table 2-41 : GPIO OEN List for SYS_IOMUX *(on page 97)* for more information.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 32

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-611 SYS IOMUX CFGSAIF SYSCFG FMUX 32 Register Description

Offset	0x80			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u0_WAVE511_i_-uart_rxsin_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_can_ctrl_rxd_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved

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Table 2-611 SYS IOMUX CFGSAIF SYSCFG FMUX 32 Register Description (continued)

Offset	0x80			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[22:16]	sys_iomux_gpi_u0_cdn_usb_over-current_n_io_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u0_cdns_spdif_spdi-fi_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 33

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-612 SYS IOMUX CFGSAIF SYSCFG FMUX 33 Register Description

Offset	0x84			
Default	**0x2**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u0_clkrst_src_by-pass_jtag_trstn_cfg	WR	0x2	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_dom_vout_-top_u0_hdmi_tx_pin_cec_sda_in_-cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u0_dom_vout_-top_u0_hdmi_tx_pin_ddc_scl_in_-cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u0_dom_vout_-top_u0_hdmi_tx_pin_ddc_sda_in_-cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFGSAIF SYSCFG FMUX 34

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-613 SYS IOMUX CFGSAIF SYSCFG FMUX 34 Register Description

Offset	**0x88**			
Default	**0x272600**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u0_dom_vout_-top_u0_hdmi_tx_pin_hpd_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_i2c_ic_clk_in_-a_cfg	WR	0x26	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u0_i2c_ic_data_in_-a_cfg	WR	0x27	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u0_sdio_card_de-tect_n_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 35

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-614 SYS IOMUX CFGSAIF SYSCFG FMUX 35 Register Description

Offset	**0x8c**			
Default	**0xb080000**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u0_sdio_card_int_-n_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved

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Table 2-614 SYS IOMUX CFGSAIF SYSCFG FMUX 35 Register Description (continued)

Offset	0x8c			
Default	**0xb080000**			
Bit	**Name**	**Access**	**Default**	**Description**
[14:8]	sys_iomux_gpi_u0_sdio_card_-write_prt_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u0_uart_sin_cfg	WR	0x8	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u0_hifi4_JTCK_cfg	WR	0xb	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 36

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-615 SYS IOMUX CFGSAIF SYSCFG FMUX 36 Register Description

Offset	0x90			
Default	**0x40f0e0c**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u0_hifi4_JTDI_cfg	WR	0xc	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_hifi4_JTMS_cfg	WR	0xe	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u0_hifi4_JTRSTn_cfg	WR	0xf	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved

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Table 2-615 SYS IOMUX CFGSAIF SYSCFG FMUX 36 Register Description (continued)

Offset	0x90			
Default	0x40f0e0c			
Bit	Name	Access	Default	Description
[30:24]	sys_iomux_gpi_u0_jtag_certification_tdi_cfg	WR	0x4	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 37

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-616 SYS IOMUX CFGSAIF SYSCFG FMUX 37 Register Description

Offset	0x94			
Default	0x6			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpi_u0_jtag_certification_tms_cfg	WR	0x6	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_pdm_4mic_dmic0_din_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u0_pdm_4mic_dmic1_din_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u0_saif_audio_sdin_mux_i2srx_ext_sdin0_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 38

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

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Table 2-617 SYS IOMUX CFGSAIF SYSCFG FMUX 38 Register Description

Offset	0x98			
Default	0x32330000			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpi_u0_saif_audio_sdin_mux_i2srx_ext_sdin1_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_saif_audio_sdin_mux_i2srx_ext_sdin2_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u0_ssp_spi_SSPCLKIN_cfg	WR	0x33	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u0_ssp_spi_SSPFSSIN_cfg	WR	0x32	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 39

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-618 SYS IOMUX CFGSAIF SYSCFG FMUX 39 Register Description

Offset	0x9c			
Default	0x334			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpi_u0_ssp_spi_SSPRXD_cfg	WR	0x34	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_sys_crg_clk_jtag_tck_cfg	WR	0x3	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved

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Table 2-618 SYS IOMUX CFGSAIF SYSCFG FMUX 39 Register Description (continued)

Offset	0x9c			
Default	**0x334**			
Bit	**Name**	**Access**	**Default**	**Description**
[22:16]	sys_iomux_gpi_u0_sys_crg_ext_m-clk_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u0_sys_crg_i2srx_b-clk_slv_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 40

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-619 SYS IOMUX CFGSAIF SYSCFG FMUX 40 Register Description

Offset	0xa0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u0_sys_crg_i2srx_lr-ck_slv_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_sys_crg_i2stx_b-clk_slv_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u0_sys_crg_i2stx_lr-ck_slv_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u0_sys_crg_tdm_-clk_slv_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFGSAIF SYSCFG FMUX 41

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-620 SYS IOMUX CFGSAIF SYSCFG FMUX 41 Register Description

Offset	**0xa4**			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u0_tdm16slot_-PCM_RXD_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u0_tdm16slot_-PCM_SYNCIN_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u1_can_ctrl_rxd_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u1_i2c_ic_clk_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 42

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-621 SYS IOMUX CFGSAIF SYSCFG FMUX 42 Register Description

Offset	**0xa8**			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u1_i2c_ic_data_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved

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Table 2-621 SYS IOMUX CFGSAIF SYSCFG FMUX 42 Register Description (continued)

Offset	0xa8			
Default	0x0			
Bit	Name	Access	Default	Description
[14:8]	sys_iomux_gpi_u1_sdio_card_detect_n_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u1_sdio_card_int_n_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u1_sdio_card_write_prt_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 43

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-622 SYS IOMUX CFGSAIF SYSCFG FMUX 43 Register Description

Offset	0xac			
Default	0x0			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpi_u1_sdio_ccmd_in_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u1_sdio_cdata_in_0_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u1_sdio_cdata_in_1_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved

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Table 2-622 SYS IOMUX CFGSAIF SYSCFG FMUX 43 Register Description (continued)

Offset	0xac			
Default	0x0			
Bit	Name	Access	Default	Description
[30:24]	sys_iomux_gpi_u1_sdio_cdata_in_-2_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 44

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-623 SYS IOMUX CFGSAIF SYSCFG FMUX 44 Register Description

Offset	0xb0			
Default	0x0			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpi_u1_sdio_cdata_in_-3_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u1_sdio_cdata_in_-4_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u1_sdio_cdata_in_-5_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u1_sdio_cdata_in_-6_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 45

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

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Table 2-624 SYS IOMUX CFGSAIF SYSCFG FMUX 45 Register Description

Offset	0xb4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u1_sdio_cdata_in_-7_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u1_sdio_data_-strobe_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u1_uart_cts_n_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u1_uart_sin_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 46

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-625 SYS IOMUX CFGSAIF SYSCFG FMUX 46 Register Description

Offset	0xb8			
Default	**0x383637**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u1_ssp_spi_SSP-CLKIN_cfg	WR	0x37	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u1_ssp_spi_-SSPFSSIN_cfg	WR	0x36	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved

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Table 2-625 SYS IOMUX CFGSAIF SYSCFG FMUX 46 Register Description (continued)

Offset	0xb8			
Default	**0x383637**			
Bit	**Name**	**Access**	**Default**	**Description**
[22:16]	sys_iomux_gpi_u1_ssp_spi_-SSPRXD_cfg	WR	0x38	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u2_i2c_ic_clk_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 47

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-626 SYS IOMUX CFGSAIF SYSCFG FMUX 47 Register Description

Offset	0xbc			
Default	**0x2a2d00**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u2_i2c_ic_data_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u2_uart_cts_n_cfg	WR	0x2d	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u2_uart_sin_cfg	WR	0x2a	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u2_ssp_spi_SSP-CLKIN_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFGSAIF SYSCFG FMUX 48

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-627 SYS IOMUX CFGSAIF SYSCFG FMUX 48 Register Description

Offset	**0xc0**			
Default	**0x29280000**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u2_ssp_spi_-SSPFSSIN_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u2_ssp_spi_-SSPRXD_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u3_i2c_ic_clk_in_-a_cfg	WR	0x28	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u3_i2c_ic_data_in_-a_cfg	WR	0x29	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 49

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-628 SYS IOMUX CFGSAIF SYSCFG FMUX 49 Register Description

Offset	**0xc4**			
Default	**0x3c3a3b15**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u3_uart_sin_cfg	WR	0x15	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved

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Table 2-628 SYS IOMUX CFGSAIF SYSCFG FMUX 49 Register Description (continued)

Offset	0xc4			
Default	**0x3c3a3b15**			
Bit	**Name**	**Access**	**Default**	**Description**
[14:8]	sys_iomux_gpi_u3_ssp_spi_SSP-CLKIN_cfg	WR	0x3b	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u3_ssp_spi_-SSPFSSIN_cfg	WR	0x3a	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u3_ssp_spi_-SSPRXD_cfg	WR	0x3c	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 50

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-629 SYS IOMUX CFGSAIF SYSCFG FMUX 50 Register Description

Offset	0xc8			
Default	**0x2e310000**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u4_i2c_ic_clk_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u4_i2c_ic_data_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u4_uart_cts_n_cfg	WR	0x31	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved

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Table 2-629 SYS IOMUX CFGSAIF SYSCFG FMUX 50 Register Description (continued)

Offset	0xc8			
Default	0x2e310000			
Bit	Name	Access	Default	Description
[30:24]	sys_iomux_gpi_u4_uart_sin_cfg	WR	0x2e	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 51

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-630 SYS IOMUX CFGSAIF SYSCFG FMUX 51 Register Description

Offset	0xcc			
Default	0x403e3f			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpi_u4_ssp_spi_SSP-CLKIN_cfg	WR	0x3f	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u4_ssp_spi_-SSPFSSIN_cfg	WR	0x3e	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u4_ssp_spi_-SSPRXD_cfg	WR	0x40	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u5_i2c_ic_clk_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 52

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

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Table 2-631 SYS IOMUX CFGSAIF SYSCFG FMUX 52 Register Description

Offset	0xd0			
Default	0x0			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpi_u5_i2c_ic_data_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u5_uart_cts_n_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u5_uart_sin_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u5_ssp_spi_SSP-CLKIN_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 53

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-632 SYS IOMUX CFGSAIF SYSCFG FMUX 53 Register Description

Offset	0xd4			
Default	0x0			
Bit	Name	Access	Default	Description
[6:0]	sys_iomux_gpi_u5_ssp_spi_-SSPFSSIN_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u5_ssp_spi_-SSPRXD_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved

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Table 2-632 SYS IOMUX CFGSAIF SYSCFG FMUX 53 Register Description (continued)

Offset	0xd4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[22:16]	sys_iomux_gpi_u6_i2c_ic_clk_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23]	Reserved	None	0x0	Reserved
[30:24]	sys_iomux_gpi_u6_i2c_ic_data_in_-a_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG FMUX 54

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-633 SYS IOMUX CFGSAIF SYSCFG FMUX 54 Register Description

Offset	0xd8			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[6:0]	sys_iomux_gpi_u6_ssp_spi_SSP-CLKIN_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7]	Reserved	None	0x0	Reserved
[14:8]	sys_iomux_gpi_u6_ssp_spi_-SSPFSSIN_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15]	Reserved	None	0x0	Reserved
[22:16]	sys_iomux_gpi_u6_ssp_spi_-SSPRXD_cfg	WR	0x0	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31:23]	Reserved	None	0x0	Reserved

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SYS IOMUX CFGSAIF SYSCFG IOIRQ 55

Table 2-634 SYS IOMUX CFGSAIF SYSCFG IOIRQ 55 Register Description

Offset	0xdc			
Default	0x0			
Bit	Name	Access	Default	Description
[0]	sys_gpioen_0_reg	WR	0x0	Enable GPIO IRQ function
[1:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG IOIRQ 56

Table 2-635 SYS IOMUX CFGSAIF SYSCFG IOIRQ 56 Register Description

Offset	0xe0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpiois_0_reg	WR	0x0	• 1: Edge trigger • 0: Level trigger

SYS IOMUX CFGSAIF SYSCFG IOIRQ 57

Table 2-636 SYS IOMUX CFGSAIF SYSCFG IOIRQ 57 Register Description

Offset	0xe4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpiois_1_reg	WR	0x0	• 1: Edge trigger • 0: Level trigger

SYS IOMUX CFGSAIF SYSCFG IOIRQ 58

Table 2-637 SYS IOMUX CFGSAIF SYSCFG IOIRQ 58 Register Description

Offset	0xe8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioic_0_reg	WR	0x0	• Do not clear the register • Clear the register

Note:
You can also write 0 and 1 sequentially to clear edge IRQ.

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SYS IOMUX CFGSAIF SYSCFG IOIRQ 59

Table 2-638 SYS IOMUX CFGSAIF SYSCFG IOIRQ 59 Register Description

Offset	0xec			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioic_1_reg	WR	0x0	• Do not clear the register • Clear the register

Note:
You can also write 0 and 1 sequentially to clear edge IRQ.

SYS IOMUX CFGSAIF SYSCFG IOIRQ 60

Table 2-639 SYS IOMUX CFGSAIF SYSCFG IOIRQ 60 Register Description

Offset	0xf0			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioibe_0_reg	WR	0x0	• Trigger on both edges • Trigger on a single edge

SYS IOMUX CFGSAIF SYSCFG IOIRQ 61

Table 2-640 SYS IOMUX CFGSAIF SYSCFG IOIRQ 61 Register Description

Offset	0xf4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioibe_1_reg	WR	0x0	• Trigger on both edges • Trigger on a single edge

SYS IOMUX CFGSAIF SYSCFG IOIRQ 62

Table 2-641 SYS IOMUX CFGSAIF SYSCFG IOIRQ 62 Register Description

Offset	0xf8			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioiev_0_reg	WR	0x0	• 1: Positive/Low • 0: Negative/High

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SYS IOMUX CFGSAIF SYSCFG IOIRQ 63

Table 2-642 SYS IOMUX CFGSAIF SYSCFG IOIRQ 63 Register Description

Offset	0xfc			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioiev_1_reg	WR	0x0	• 1: Positive/Low • 0: Negative/High

SYS IOMUX CFGSAIF SYSCFG IOIRQ 64

Table 2-643 SYS IOMUX CFGSAIF SYSCFG IOIRQ 64 Register Description

Offset	0x100			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioie_0_reg	WR	0x0	• 1: Unmask • 0: Mask

SYS IOMUX CFGSAIF SYSCFG IOIRQ 65

Table 2-644 SYS IOMUX CFGSAIF SYSCFG IOIRQ 65 Register Description

Offset	0x104			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioie_1_reg	WR	0x0	• 1: Unmask • 0: Mask

SYS IOMUX CFGSAIF SYSCFG IOIRQ 66

Table 2-645 SYS IOMUX CFGSAIF SYSCFG IOIRQ 66 Register Description

Offset	0x108			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioris_0_reg	RO	0x0	Status of the edge trigger. The register can be cleared by writing gpio ic.

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SYS IOMUX CFGSAIF SYSCFG IOIRQ 67

Table 2-646 SYS IOMUX CFGSAIF SYSCFG IOIRQ 67 Register Description

Offset	0x10c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpioris_1_reg	RO	0x0	Status of the edge trigger. The register can be cleared by writing gpio ic.

SYS IOMUX CFGSAIF SYSCFG IOIRQ 68

Table 2-647 SYS IOMUX CFGSAIF SYSCFG IOIRQ 68 Register Description

Offset	0x110			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpiomis_0_reg	RO	0x0	The masked GPIO IRQ status

SYS IOMUX CFGSAIF SYSCFG IOIRQ 69

Table 2-648 SYS IOMUX CFGSAIF SYSCFG IOIRQ 69 Register Description

Offset	0x114			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpiomis_1_reg	RO	0x0	The masked GPIO IRQ status

SYS IOMUX CFGSAIF SYSCFG IOIRQ 70

Table 2-649 SYS IOMUX CFGSAIF SYSCFG IOIRQ 70 Register Description

Offset	0x118			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpio_in_sync2_0_reg	RO	0x0	Status of the gpio_in after synchronization

SYS IOMUX CFGSAIF SYSCFG IOIRQ 71

Table 2-650 SYS IOMUX CFGSAIF SYSCFG IOIRQ 71 Register Description

Offset	0x11c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:31]	sys_gpio_in_sync2_1_reg	RO	0x0	Status of the gpio_in after synchronization

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SYS IOMUX CFG SAIF SYSCFG 288

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-651 SYS IOMUX CFG SAIF SYSCFG 288 Register Description

Offset	**0x120**			
Default	**0x11**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO0_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO0_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO0_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO0_PD	WR	0x1	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO0_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO0_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO0_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 292

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-652 SYS IOMUX CFG SAIF SYSCFG 292 Register Description

Offset	**0x124**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO1_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO1_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO1_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO1_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO1_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO1_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO1_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 296

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-653 SYS IOMUX CFG SAIF SYSCFG 296 Register Description

Offset	**0x128**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO2_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO2_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO2_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO2_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO2_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO2_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO2_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 300

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-654 SYS IOMUX CFG SAIF SYSCFG 300 Register Description

Offset	**0x12c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO3_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO3_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO3_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO3_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO3_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO3_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO3_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 304

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-655 SYS IOMUX CFG SAIF SYSCFG 304 Register Description

Offset	**0x130**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO4_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO4_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO4_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO4_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO4_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO4_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO4_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 308

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-656 SYS IOMUX CFG SAIF SYSCFG 308 Register Description

Offset	**0x134**			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO5_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO5_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO5_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO5_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO5_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO5_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO5_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 312

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-657 SYS IOMUX CFG SAIF SYSCFG 312 Register Description

Offset	**0x138**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO6_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO6_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO6_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO6_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO6_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO6_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO6_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 316

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-658 SYS IOMUX CFG SAIF SYSCFG 316 Register Description

Offset	**0x13c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO7_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO7_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO7_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO7_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO7_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO7_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO7_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 320

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-659 SYS IOMUX CFG SAIF SYSCFG 320 Register Description

Offset	**0x140**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO8_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO8_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO8_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO8_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO8_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO8_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO8_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 324

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-660 SYS IOMUX CFG SAIF SYSCFG 324 Register Description

Offset	**0x144**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO9_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO9_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO9_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO9_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO9_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO9_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO9_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 328

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-661 SYS IOMUX CFG SAIF SYSCFG 328 Register Description

Offset	**0x148**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO10_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO10_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO10_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO10_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO10_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO10_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO10_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 332

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-662 SYS IOMUX CFG SAIF SYSCFG 332 Register Description

Offset	**0x14c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO11_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO11_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO11_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO11_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO11_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO11_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO11_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 336

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-663 SYS IOMUX CFG SAIF SYSCFG 336 Register Description

Offset	**0x150**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO12_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO12_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO12_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO12_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO12_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO12_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO12_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 340

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-664 SYS IOMUX CFG SAIF SYSCFG 340 Register Description

Offset	**0x154**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO13_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO13_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO13_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO13_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO13_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO13_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO13_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 344

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-665 SYS IOMUX CFG SAIF SYSCFG 344 Register Description

Offset	**0x158**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO14_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO14_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO14_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO14_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO14_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO14_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO14_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 348

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-666 SYS IOMUX CFG SAIF SYSCFG 348 Register Description

Offset	**0x15c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO15_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO15_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO15_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO15_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO15_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO15_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO15_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 352

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-667 SYS IOMUX CFG SAIF SYSCFG 352 Register Description

Offset	**0x160**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO16_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO16_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO16_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO16_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO16_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO16_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO16_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 356

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-668 SYS IOMUX CFG SAIF SYSCFG 356 Register Description

Offset	**0x164**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO17_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO17_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO17_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO17_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO17_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO17_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO17_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 360

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-669 SYS IOMUX CFG SAIF SYSCFG 360 Register Description

Offset	**0x168**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO18_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO18_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO18_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO18_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO18_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO18_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO18_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 364

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-670 SYS IOMUX CFG SAIF SYSCFG 364 Register Description

Offset	**0x16c**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO19_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO19_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO19_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO19_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO19_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO19_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO19_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 368

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-671 SYS IOMUX CFG SAIF SYSCFG 368 Register Description

Offset	**0x170**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO20_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO20_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO20_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO20_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO20_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO20_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO20_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 372

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-672 SYS IOMUX CFG SAIF SYSCFG 372 Register Description

Offset	**0x174**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO21_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO21_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO21_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO21_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO21_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO21_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO21_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 376

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-673 SYS IOMUX CFG SAIF SYSCFG 376 Register Description

Offset	**0x178**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO22_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO22_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO22_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO22_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO22_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO22_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO22_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 380

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-674 SYS IOMUX CFG SAIF SYSCFG 380 Register Description

Offset	**0x17c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO23_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO23_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO23_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO23_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO23_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO23_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO23_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 384

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-675 SYS IOMUX CFG SAIF SYSCFG 384 Register Description

Offset	**0x180**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO24_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO24_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO24_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO24_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO24_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO24_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO24_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 388

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-676 SYS IOMUX CFG SAIF SYSCFG 388 Register Description

Offset	**0x184**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO25_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO25_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO25_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO25_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO25_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO25_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO25_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 392

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-677 SYS IOMUX CFG SAIF SYSCFG 392 Register Description

Offset	**0x188**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO26_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO26_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO26_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO26_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO26_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO26_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO26_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 396

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-678 SYS IOMUX CFG SAIF SYSCFG 396 Register Description

Offset	**0x18c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO27_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO27_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO27_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO27_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO27_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO27_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO27_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 400

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-679 SYS IOMUX CFG SAIF SYSCFG 400 Register Description

Offset	**0x190**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO28_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO28_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO28_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO28_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO28_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO28_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO28_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 404

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-680 SYS IOMUX CFG SAIF SYSCFG 404 Register Description

Offset	**0x194**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO29_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO29_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO29_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO29_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO29_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO29_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO29_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 408

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-681 SYS IOMUX CFG SAIF SYSCFG 408 Register Description

Offset	**0x198**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO30_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO30_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO30_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO30_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO30_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO30_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO30_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 412

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-682 SYS IOMUX CFG SAIF SYSCFG 412 Register Description

Offset	**0x19c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO31_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO31_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO31_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO31_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO31_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO31_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO31_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 416

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-683 SYS IOMUX CFG SAIF SYSCFG 416 Register Description

Offset	**0x1a0**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO32_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO32_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO32_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO32_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO32_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO32_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO32_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 420

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-684 SYS IOMUX CFG SAIF SYSCFG 420 Register Description

Offset	**0x1a4**			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO33_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO33_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO33_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO33_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO33_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO33_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO33_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 424

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-685 SYS IOMUX CFG SAIF SYSCFG 424 Register Description

Offset	**0x1a8**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO34_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO34_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO34_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO34_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO34_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO34_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO34_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 428

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-686 SYS IOMUX CFG SAIF SYSCFG 428 Register Description

Offset	**0x1ac**			
Default	**0x11**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO35_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO35_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO35_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO35_PD	WR	0x1	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO35_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO35_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO35_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 432

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-687 SYS IOMUX CFG SAIF SYSCFG 432 Register Description

Offset	**0x1b0**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO36_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO36_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO36_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO36_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO36_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO36_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO36_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 436

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-688 SYS IOMUX CFG SAIF SYSCFG 436 Register Description

Offset	**0x1b4**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO37_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO37_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO37_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO37_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO37_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO37_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO37_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 440

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-689 SYS IOMUX CFG SAIF SYSCFG 440 Register Description

Offset	**0x1b8**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO38_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO38_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO38_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO38_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO38_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO38_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO38_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 444

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-690 SYS IOMUX CFG SAIF SYSCFG 444 Register Description

Offset	**0x1bc**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO39_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO39_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO39_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO39_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO39_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO39_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO39_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 448

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-691 SYS IOMUX CFG SAIF SYSCFG 448 Register Description

Offset	**0x1c0**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO40_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO40_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO40_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO40_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO40_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO40_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO40_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 452

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-692 SYS IOMUX CFG SAIF SYSCFG 452 Register Description

Offset	**0x1c4**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO41_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO41_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO41_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO41_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO41_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO41_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO41_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 456

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-693 SYS IOMUX CFG SAIF SYSCFG 456 Register Description

Offset	**0x1c8**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO42_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO42_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO42_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO42_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO42_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO42_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO42_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 460

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-694 SYS IOMUX CFG SAIF SYSCFG 460 Register Description

Offset	**0x1cc**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO43_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO43_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO43_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO43_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO43_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO43_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO43_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 464

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-695 SYS IOMUX CFG SAIF SYSCFG 464 Register Description

Offset	**0x1d0**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO44_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO44_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO44_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO44_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO44_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO44_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO44_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 468

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-696 SYS IOMUX CFG SAIF SYSCFG 468 Register Description

Offset	**0x1d4**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO45_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO45_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO45_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO45_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO45_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO45_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO45_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 472

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-697 SYS IOMUX CFG SAIF SYSCFG 472 Register Description

Offset	**0x1d8**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO46_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO46_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO46_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO46_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO46_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO46_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO46_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 476

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-698 SYS IOMUX CFG SAIF SYSCFG 476 Register Description

Offset	**0x1dc**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO47_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO47_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO47_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO47_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO47_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO47_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO47_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 480

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-699 SYS IOMUX CFG SAIF SYSCFG 480 Register Description

Offset	**0x1e0**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO48_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO48_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO48_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO48_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO48_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO48_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO48_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 484

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-700 SYS IOMUX CFG SAIF SYSCFG 484 Register Description

Offset	**0x1e4**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO49_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO49_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO49_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO49_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO49_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO49_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO49_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 488

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-701 SYS IOMUX CFG SAIF SYSCFG 488 Register Description

Offset	**0x1e8**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO50_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO50_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO50_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO50_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO50_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO50_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO50_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 492

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-702 SYS IOMUX CFG SAIF SYSCFG 492 Register Description

Offset	**0x1ec**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO51_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO51_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO51_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO51_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO51_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO51_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO51_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 496

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-703 SYS IOMUX CFG SAIF SYSCFG 496 Register Description

Offset	**0x1f0**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO52_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO52_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO52_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO52_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO52_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO52_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO52_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 500

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-704 SYS IOMUX CFG SAIF SYSCFG 500 Register Description

Offset	**0x1f4**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO53_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO53_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO53_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO53_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO53_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO53_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO53_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 504

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-705 SYS IOMUX CFG SAIF SYSCFG 504 Register Description

Offset	**0x1f8**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO54_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO54_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO54_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO54_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO54_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO54_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO54_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 508

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-706 SYS IOMUX CFG SAIF SYSCFG 508 Register Description

Offset	**0x1fc**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO55_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO55_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO55_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO55_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO55_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO55_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO55_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 512

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-707 SYS IOMUX CFG SAIF SYSCFG 512 Register Description

Offset	**0x200**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO56_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO56_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO56_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO56_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO56_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO56_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO56_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 516

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-708 SYS IOMUX CFG SAIF SYSCFG 516 Register Description

Offset	**0x204**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO57_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO57_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO57_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO57_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO57_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO57_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO57_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 520

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-709 SYS IOMUX CFG SAIF SYSCFG 520 Register Description

Offset	**0x208**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO58_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO58_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO58_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO58_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO58_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO58_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO58_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 524

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-710 SYS IOMUX CFG SAIF SYSCFG 524 Register Description

Offset	**0x20c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO59_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO59_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO59_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO59_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO59_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO59_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO59_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 528

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-711 SYS IOMUX CFG SAIF SYSCFG 528 Register Description

Offset	**0x210**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO60_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO60_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO60_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO60_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO60_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO60_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO60_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 532

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-712 SYS IOMUX CFG SAIF SYSCFG 532 Register Description

Offset	**0x214**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO61_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO61_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO61_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO61_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO61_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO61_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO61_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 536

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-713 SYS IOMUX CFG SAIF SYSCFG 536 Register Description

Offset	**0x218**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO62_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO62_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO62_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO62_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO62_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO62_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO62_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 540

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-714 SYS IOMUX CFG SAIF SYSCFG 540 Register Description

Offset	**0x21c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_GPIO63_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_GPIO63_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_GPIO63_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_GPIO63_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_GPIO63_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_GPIO63_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_GPIO63_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 544

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_CLK".

Table 2-715 SYS IOMUX CFG SAIF SYSCFG 544 Register Description

Offset	**0x220**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_CLK_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_CLK_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_CLK_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_CLK_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_CLK_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_CLK_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_CLK_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 548

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_CMD".

Table 2-716 SYS IOMUX CFG SAIF SYSCFG 548 Register Description

Offset	**0x224**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_CMD_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_CMD_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_CMD_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_CMD_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_CMD_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_CMD_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_CMD_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 552

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_DATA0".

Table 2-717 SYS IOMUX CFG SAIF SYSCFG 552 Register Description

Offset	**0x228**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_DATA0_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_DATA0_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_DATA0_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_DATA0_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_DATA0_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_DATA0_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_DATA0_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 556

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_DATA1".

Table 2-718 SYS IOMUX CFG SAIF SYSCFG 556 Register Description

Offset	**0x22c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_DATA1_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_DATA1_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_DATA1_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_DATA1_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_DATA1_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_DATA1_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_DATA1_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 560

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_DATA2".

Table 2-719 SYS IOMUX CFG SAIF SYSCFG 560 Register Description

Offset	**0x230**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_DATA2_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_DATA2_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_DATA2_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_DATA2_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_DATA2_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_DATA2_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_DATA2_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 564

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_DATA3".

Table 2-720 SYS IOMUX CFG SAIF SYSCFG 564 Register Description

Offset	**0x234**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_DATA3_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_DATA3_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_DATA3_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_DATA3_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_DATA3_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_DATA3_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_DATA3_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 568

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_DATA4".

Table 2-721 SYS IOMUX CFG SAIF SYSCFG 568 Register Description

Offset	**0x238**			
Default	**0x9**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_DATA4_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_DATA4_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_DATA4_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_DATA4_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_DATA4_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_DATA4_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_DATA4_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 572

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_DATA5".

Table 2-722 SYS IOMUX CFG SAIF SYSCFG 572 Register Description

Offset	**0x23c**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_DATA5_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_DATA5_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_DATA5_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_DATA5_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_DATA5_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_DATA5_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_DATA5_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 576

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_DATA6".

Table 2-723 SYS IOMUX CFG SAIF SYSCFG 576 Register Description

Offset	**0x240**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_DATA6_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_DATA6_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_DATA6_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_DATA6_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_DATA6_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_DATA6_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_DATA6_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 580

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_DATA7".

Table 2-724 SYS IOMUX CFG SAIF SYSCFG 580 Register Description

Offset	**0x244**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_DATA7_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_DATA7_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_DATA7_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_DATA7_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_DATA7_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_DATA7_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_DATA7_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 584

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "SD0_STRB".

Table 2-725 SYS IOMUX CFG SAIF SYSCFG 584 Register Description

Offset	**0x248**			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_SD0_STRB_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_SD0_STRB_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_SD0_STRB_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_SD0_STRB_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_SD0_STRB_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_SD0_STRB_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_SD0_STRB_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 588

Table 2-726 SYS IOMUX CFG SAIF SYSCFG 588 Register Description

Offset	0x24c			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_MDC_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 592

Table 2-727 SYS IOMUX CFG SAIF SYSCFG 592 Register Description

Offset	0x250			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_MDIO_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 596

Table 2-728 SYS IOMUX CFG SAIF SYSCFG 596 Register Description

Offset	0x254			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_RXD0_-syscon	WR	0x2	• [1:0] = 0 : GMAC1 IO voltage select 3.3 V • [1:0] = 1: GMAC1 IO voltage select 2.5 V • [1:0] = 2: GMAC1 IO voltage select 1.8 V
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 600

Table 2-729 SYS IOMUX CFG SAIF SYSCFG 600 Register Description

Offset	0x258			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_RXD1_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 604

Table 2-730 SYS IOMUX CFG SAIF SYSCFG 604 Register Description

Offset	0x25c			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_RXD2_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 608

Table 2-731 SYS IOMUX CFG SAIF SYSCFG 608 Register Description

Offset	0x260			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_RXD3_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 612

Table 2-732 SYS IOMUX CFG SAIF SYSCFG 612 Register Description

Offset	0x264			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_RXDV_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 616

Table 2-733 SYS IOMUX CFG SAIF SYSCFG 616 Register Description

Offset	0x268			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_RXC_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 620

Table 2-734 SYS IOMUX CFG SAIF SYSCFG 620 Register Description

Offset	0x26c			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_TXD0_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 624

Table 2-735 SYS IOMUX CFG SAIF SYSCFG 624 Register Description

Offset	0x270			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_TXD1_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 628

Table 2-736 SYS IOMUX CFG SAIF SYSCFG 628 Register Description

Offset	0x274			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_TXD2_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 632

Table 2-737 SYS IOMUX CFG SAIF SYSCFG 632 Register Description

Offset	0x278			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_TXD3_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

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SYS IOMUX CFG SAIF SYSCFG 636

Table 2-738 SYS IOMUX CFG SAIF SYSCFG 636 Register Description

Offset	0x27c			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_TXEN_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 640

Table 2-739 SYS IOMUX CFG SAIF SYSCFG 640 Register Description

Offset	0x280			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC1_TXC_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 644

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "QSPI_SCLK".

Table 2-740 SYS IOMUX CFG SAIF SYSCFG 644 Register Description

Offset	0x284			
Default	0x1			
Bit	Name	Access	Default	Description
[0]	PADCFG_PAD_QSPI_SCLK_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_QSPI_SCLK_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_QSPI_SCLK_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No

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Table 2-740 SYS IOMUX CFG SAIF SYSCFG 644 Register Description (continued)

Offset	0x284			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[4]	PADCFG_PAD_QSPI_SCLK_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_QSPI_SCLK_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_QSPI_SCLK_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_QSPI_SCLK_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 648

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "QSPI_CSn0".

Table 2-741 SYS IOMUX CFG SAIF SYSCFG 648 Register Description

Offset	0x288			
Default	**0x8**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_QSPI_CSn0_IE	WR	0x0	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_QSPI_CSn0_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA.

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Table 2-741 SYS IOMUX CFG SAIF SYSCFG 648 Register Description (continued)

Offset	0x288			
Default	**0x8**			
Bit	**Name**	**Access**	**Default**	**Description**
				• 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_QSPI_CSn0_PU	WR	0x1	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_QSPI_CSn0_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_QSPI_CSn0_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_QSPI_CSn0_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_QSPI_CSn0_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 652

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "QSPI_DATA0".

Table 2-742 SYS IOMUX CFG SAIF SYSCFG 652 Register Description

Offset	0x28c			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_QSPI_DATA0_IE	WR	0x1	*Input Enable (IE)* Controller:

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Table 2-742 SYS IOMUX CFG SAIF SYSCFG 652 Register Description (continued)

Offset	0x28c			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
				• 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_QSPI_DATA0_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_QSPI_DATA0_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_QSPI_DATA0_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_QSPI_DATA0_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_QSPI_DATA0_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_QSPI_DATA0_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 656

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "QSPI_DATA1".

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Table 2-743 SYS IOMUX CFG SAIF SYSCFG 656 Register Description

Offset	0x290			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_QSPI_DATA1_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_QSPI_DATA1_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_QSPI_DATA1_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_QSPI_DATA1_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_QSPI_DATA1_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_QSPI_DATA1_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_QSPI_DATA1_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 660

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "QSPI_DATA2".

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Table 2-744 SYS IOMUX CFG SAIF SYSCFG 660 Register Description

Offset	0x294			
Default	0x1			
Bit	Name	Access	Default	Description
[0]	PADCFG_PAD_QSPI_DATA2_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_QSPI_DATA2_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_QSPI_DATA2_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_QSPI_DATA2_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_QSPI_DATA2_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_QSPI_DATA2_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_QSPI_DATA2_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFG SAIF SYSCFG 664

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

In this case, the signal name is "QSPI_DATA3".

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Table 2-745 SYS IOMUX CFG SAIF SYSCFG 664 Register Description

Offset	0x298			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_QSPI_DATA3_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_QSPI_DATA3_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_QSPI_DATA3_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_QSPI_DATA3_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_QSPI_DATA3_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_QSPI_DATA3_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_QSPI_DATA3_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG 668

The register can be used to configure the function selector of the system signal indicated in the "Name" column. For example, "PAD_GMAC1_RXC_func_sel" indicates the function selector of the signal "GMAC1_RXC".

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Table 2-746 SYS IOMUX CFGSAIF SYSCFG 668 Register Description

Offset	0x29c			
Default	0x0			
Bit	Name	Access	Default	Description
[1:0]	PAD_GMAC1_RXC_func_sel	WR	0x0	Function selector of GMAC1_RXC: • Function 0: u0_sys_crg.clk_gmac1_rgmii_rx • Function 1: u0_sys_crg.clk_gmac1_rmii_ref • Function 2: None • Function 3: None
[4:2]	PAD_GPIO10_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[7:5]	PAD_GPIO11_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[10:8]	PAD_GPIO12_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[13:11]	PAD_GPIO13_func_sel	WR	0x0	GPIO function selector:

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Table 2-746 SYS IOMUX CFGSAIF SYSCFG 668 Register Description (continued)

Offset	0x29c			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[16:14]	PAD_GPIO14_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[19:17]	PAD_GPIO15_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[22:20]	PAD_GPIO16_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[25:23]	PAD_GPIO17_func_sel	WR	0x0	GPIO function selector:

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Table 2-746 SYS IOMUX CFGSAIF SYSCFG 668 Register Description (continued)

Offset	0x29c			
Default	0x0			
Bit	Name	Access	Default	Description
				• Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[28:26]	PAD_GPIO18_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[31:29]	PAD_GPIO19_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.

SYS IOMUX CFGSAIF SYSCFG 672

Table 2-747 SYS IOMUX CFGSAIF SYSCFG 672 Register Description

Offset	0x2a0			
Default	0x0			
Bit	Name	Access	Default	Description
[2:0]	PAD_GPIO20_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-747 SYS IOMUX CFGSAIF SYSCFG 672 Register Description (continued)

Offset	0x2a0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[5:3]	PAD_GPIO21_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[8:6]	PAD_GPIO22_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[11:9]	PAD_GPIO23_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[14:12]	PAD_GPIO24_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-747 SYS IOMUX CFGSAIF SYSCFG 672 Register Description (continued)

Offset	0x2a0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[17:15]	PAD_GPIO25_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[20:18]	PAD_GPIO26_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[23:21]	PAD_GPIO27_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[26:24]	PAD_GPIO28_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-747 SYS IOMUX CFGSAIF SYSCFG 672 Register Description (continued)

Offset	0x2a0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[29:27]	PAD_GPIO29_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[30:31]	Reserved	None	0x0	Reserved

SYS IOMUX CFGSAIF SYSCFG 676

Table 2-748 SYS IOMUX CFGSAIF SYSCFG 676 Register Description

Offset	0x2a4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[2:0]	PAD_GPIO30_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[5:3]	PAD_GPIO31_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-748 SYS IOMUX CFGSAIF SYSCFG 676 Register Description (continued)

Offset	0x2a4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[8:6]	PAD_GPIO32_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[11:9]	PAD_GPIO33_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[14:12]	PAD_GPIO34_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[16:15]	PAD_GPIO35_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-748 SYS IOMUX CFGSAIF SYSCFG 676 Register Description (continued)

Offset	0x2a4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[19:17]	PAD_GPIO36_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[22:20]	PAD_GPIO37_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[25:23]	PAD_GPIO38_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[28:26]	PAD_GPIO39_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-748 SYS IOMUX CFGSAIF SYSCFG 676 Register Description (continued)

Offset	0x2a4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[31:29]	PAD_GPIO40_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.

SYS IOMUX CFGSAIF SYSCFG 680

Table 2-749 SYS IOMUX CFGSAIF SYSCFG 680 Register Description

Offset	0x2a8			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[2:0]	PAD_GPIO41_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[5:3]	PAD_GPIO42_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-749 SYS IOMUX CFGSAIF SYSCFG 680 Register Description (continued)

Offset	0x2a8			
Default	0x0			
Bit	Name	Access	Default	Description
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[8:6]	PAD_GPIO43_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[11:9]	PAD_GPIO44_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[14:12]	PAD_GPIO45_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[17:15]	PAD_GPIO46_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-749 SYS IOMUX CFGSAIF SYSCFG 680 Register Description (continued)

Offset	0x2a8			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[20:18]	PAD_GPIO47_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[23:21]	PAD_GPIO48_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[26:24]	PAD_GPIO49_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[29:27]	PAD_GPIO50_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-749 SYS IOMUX CFGSAIF SYSCFG 680 Register Description (continued)

Offset	0x2a8			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[30:31]	PAD_GPIO51_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.

SYS IOMUX CFGSAIF SYSCFG 684

Table 2-750 SYS IOMUX CFGSAIF SYSCFG 684 Register Description

Offset	0x2ac			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[1:0]	PAD_GPIO52_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[2:3]	PAD_GPIO53_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-750 SYS IOMUX CFGSAIF SYSCFG 684 Register Description (continued)

Offset	0x2ac			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[4:5]	PAD_GPIO54_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[8:6]	PAD_GPIO55_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[11:9]	PAD_GPIO56_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[14:12]	PAD_GPIO57_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-750 SYS IOMUX CFGSAIF SYSCFG 684 Register Description (continued)

Offset	0x2ac			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[17:15]	PAD_GPIO58_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[20:18]	PAD_GPIO59_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[23:21]	PAD_GPIO60_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[26:24]	PAD_GPIO61_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-750 SYS IOMUX CFGSAIF SYSCFG 684 Register Description (continued)

Offset	0x2ac			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[29:27]	PAD_GPIO62_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[30:31]	PAD_GPIO63_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.

SYS IOMUX CFGSAIF SYSCFG 688

Table 2-751 SYS IOMUX CFGSAIF SYSCFG 688 Register Description

Offset	0x2b0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[1:0]	PAD_GPIO6_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information.

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Table 2-751 SYS IOMUX CFGSAIF SYSCFG 688 Register Description (continued)

Offset	0x2b0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
				• Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[4:2]	PAD_GPIO7_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[7:5]	PAD_GPIO8_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[10:8]	PAD_GPIO9_func_sel	WR	0x0	GPIO function selector: • Function 0: See Function Description *(on page 84)* for more information. • Function 1: See Full Multiplexing *(on page 90)* for more information. • Function 2: See Function 2 *(on page)* for more information. • Function 3: See Function 3 *(on page)* for more information.
[13:11]	u0_dom_isp_top_u0_vin_dvp_data_c0_func_sel	WR	0x0	Function selector of DVP_DATA[0], see Function 2 *(on page)* for more information.
[16:14]	u0_dom_isp_top_u0_vin_dvp_data_c10_func_sel	WR	0x0	Function selector of DVP_DATA[10], see Function 2 *(on page)* for more information.
[19:17]	u0_dom_isp_top_u0_vin_dvp_data_c11_func_sel	WR	0x0	Function selector of DVP_DATA[11], see Function 2 *(on page)* for more information.

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Table 2-751 SYS IOMUX CFGSAIF SYSCFG 688 Register Description (continued)

Offset	0x2b0			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[22:20]	u0_dom_isp_top_u0_vin_dvp_data_c1_func_sel	WR	0x0	Function selector of DVP_DATA[1], see Function 2 *(on page)* for more information.
[25:23]	u0_dom_isp_top_u0_vin_dvp_data_c2_func_sel	WR	0x0	Function selector of DVP_DATA[2], see Function 2 *(on page)* for more information.
[28:26]	u0_dom_isp_top_u0_vin_dvp_data_c3_func_sel	WR	0x0	Function selector of DVP_DATA[3], see Function 2 *(on page)* for more information.
[31:29]	u0_dom_isp_top_u0_vin_dvp_data_c4_func_sel	WR	0x0	Function selector of DVP_DATA[4], see Function 2 *(on page)* for more information.

SYS IOMUX CFGSAIF SYSCFG 692

Table 2-752 SYS IOMUX CFGSAIF SYSCFG 692 Register Description

Offset	0x2b4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[2:0]	u0_dom_isp_top_u0_vin_dvp_data_c5_func_sel	WR	0x0	Function selector of DVP_DATA[5], see Function 2 *(on page)* for more information.
[5:3]	u0_dom_isp_top_u0_vin_dvp_data_c6_func_sel	WR	0x0	Function selector of DVP_DATA[6], see Function 2 *(on page)* for more information.
[8:6]	u0_dom_isp_top_u0_vin_dvp_data_c7_func_sel	WR	0x0	Function selector of DVP_DATA[7], see Function 2 *(on page)* for more information.
[11:9]	u0_dom_isp_top_u0_vin_dvp_data_c8_func_sel	WR	0x0	Function selector of DVP_DATA[8], see Function 2 *(on page)* for more information.
[14:12]	u0_dom_isp_top_u0_vin_dvp_data_c9_func_sel	WR	0x0	Function selector of DVP_DATA[9], see Function 2 *(on page)* for more information.
[17:15]	u0_dom_isp_top_u0_vin_dvp_hvalid_c_func_sel	WR	0x0	Function selector of DVP_HSYNC, see Function 2 *(on page)* for more information.
[20:18]	u0_dom_isp_top_u0_vin_dvp_vvalid_c_func_sel	WR	0x0	Function selector of DVP_VSYNC, see Function 2 *(on page)* for more information.
[23:21]	u0_sys_crg_dvp_clk_func_sel	WR	0x0	Function selector of DVP_CLK, see Function 2 *(on page)* for more information.
[31:24]	Reserved	None	0x0	Reserved

2.8.8. AON IOMUX CFG

The JH-7110 system provides the following AON IOMUX CFG registers for Always-ON (AON) IO multiplexing configuration.

AON IOMUX CFGSAIF SYSCFG FMUX 0

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO0 - GPIO3.

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Table 2-753 AON_SYSCONSAIF__SYSCFG_0 Register Description

Offset	0x0			
Default	0x1010101			
Bit	Name	Access	Default	Description
[2:0]	aon_iomux_gpo0_doen_cfg	WR	0x1	The selected OEN signal for GPIO0. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-5. See Table 2-42 : GPIO OEN List for AON_IOMUX *(on page 106)* for more information.
[7:3]	Reserved	None	0x0	Reserved
[10:8]	aon_iomux_gpo1_doen_cfg	WR	0x1	The selected OEN signal for GPIO1. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-5. See Table 2-42 : GPIO OEN List for AON_IOMUX *(on page 106)* for more information.
[15:11]	Reserved	None	0x0	Reserved
[18:16]	aon_iomux_gpo2_doen_cfg	WR	0x1	The selected OEN signal for GPIO2. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-5. See Table 2-42 : GPIO OEN List for AON_IOMUX *(on page 106)* for more information.
[23:19]	Reserved	None	0x0	Reserved
[26:24]	aon_iomux_gpo3_doen_cfg	WR	0x1	The selected OEN signal for GPIO3. The register value indicates the selected GPIO *(Output Enable) OEN* index from GPIO OEN list 0-5. See Table 2-42 : GPIO OEN List for AON_IOMUX *(on page 106)* for more information.
[31:27]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG FMUX 1

The register can be used to configure the selected *(Output Enable) OEN* signal for GPIO0 - GPIO3.

Table 2-754 AON IOMUX CFGSAIF SYSCFG FMUX 1 Register Description

Offset	0x4			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_iomux_gpo0_dout_cfg	WR	0x0	The selected OEN signal for GPIO0. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-9. See Table 2-42 : GPIO OEN List for AON_IOMUX *(on page 106)* for more information.
[4:7]	Reserved	None	0x0	Reserved

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Table 2-754 AON IOMUX CFGSAIF SYSCFG FMUX 1 Register Description (continued)

Offset	0x4			
Default	**0x0**			
Bit	**Name**	**Access**	**Default**	**Description**
[11:8]	aon_iomux_gpo1_dout_cfg	WR	0x0	The selected OEN signal for GPIO1. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-9. See Table 2-42 : GPIO OEN List for AON_IOMUX *(on page 106)* for more information.
[15:12]	Reserved	None	0x0	Reserved
[19:16]	aon_iomux_gpo2_dout_cfg	WR	0x0	The selected OEN signal for GPIO2. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-9. See Table 2-42 : GPIO OEN List for AON_IOMUX *(on page 106)* for more information.
[23:20]	Reserved	None	0x0	Reserved
[27:24]	aon_iomux_gpo3_dout_cfg	WR	0x0	The selected OEN signal for GPIO3. The register value indicates the selected GPIO output signal index from GPIO output signal list 0-9. See Table 2-42 : GPIO OEN List for AON_IOMUX *(on page 106)* for more information.
[31:28]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG FMUX 2

The register can be used to configure the selected GPIO connector number for input signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, name "sys_iomux_gpi_u0_WAVE511_i_uart_rxsin_cfg" indicates the corresponding input signal is "u0_WAVE511.i_uart_rxsin". See GPIO Input Signals *(on page 107)* for a complete list of the input GPIO signals.

Table 2-755 AON IOMUX CFGSAIF SYSCFG FMUX 2 Register Description

Offset	0x8			
Default	**0x5040302**			
Bit	**Name**	**Access**	**Default**	**Description**
[2:0]	aon_iomux_gpi_u0_pmu_io_event_stub_gpio_wakeup_0_cfg	WR	0x2	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[7:3]	Reserved	None	0x0	Reserved
[10:8]	aon_iomux_gpi_u0_pmu_io_event_stub_gpio_wakeup_1_cfg	WR	0x3	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[15:11]	Reserved	None	0x0	Reserved

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Table 2-755 AON IOMUX CFGSAIF SYSCFG FMUX 2 Register Description (continued)

Offset	0x8			
Default	0x5040302			
Bit	Name	Access	Default	Description
[18:16]	aon_iomux_gpi_u0_pmu_io_event_stub_gpio_wakeup_2_cfg	WR	0x4	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[23:19]	Reserved	None	0x0	Reserved
[26:24]	aon_iomux_gpi_u0_pmu_io_event_stub_gpio_wakeup_3_cfg	WR	0x5	The register value indicates the selected GPIO number + 2 (GPIO2 - GPIO63, GPIO0 and GPIO1 are not available) for the input signal.
[31:27]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG FMUX 3

Table 2-756 AON IOMUX CFGSAIF SYSCFG IOIRQ 3 Register Description

Offset	0xc			
Default	0x0			
Bit	Name	Access	Default	Description
[0]	aon_gpioen_0_reg	WR	0x0	Enable GPIO IRQ function
[1:31]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG IOIRQ 4

Table 2-757 AON IOMUX CFGSAIF SYSCFG IOIRQ 4 Register Description

Offset	0x10			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_gpiois_0_reg	WR	0x0	• 1: Edge trigger • 0: Level trigger
[4:31]	Reserved	None	0x0	Reserved

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AON IOMUX CFGSAIF SYSCFG IOIRQ 5

Table 2-758 AON IOMUX CFGSAIF SYSCFG IOIRQ 5 Register Description

Offset	0x14			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_gpioic_0_reg	WR	0x0	• 1: Do not clear the register • 0: Clear the register
[4:31]	Reserved	None	0x0	Reserved

Note:
You can write 0 and 1 in aon_gpioic_0_reg sequentially to clear edge IRQ.

AON IOMUX CFGSAIF SYSCFG IOIRQ 6

Table 2-759 AON IOMUX CFGSAIF SYSCFG IOIRQ 6 Register Description

Offset	0x18			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_gpioibe_0_reg	WR	0x0	• 1: Trigger on both edges • 0: Trigger on a single edge
[4:31]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG IOIRQ 7

Table 2-760 AON IOMUX CFGSAIF SYSCFG IOIRQ 7 Register Description

Offset	0x1c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_gpioiev_0_reg	WR	0x0	• 1: Positive/Low • 0: Negative/High
[4:31]	Reserved	None	0x0	Reserved

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AON IOMUX CFGSAIF SYSCFG IOIRQ 8

Table 2-761 AON IOMUX CFGSAIF SYSCFG IOIRQ 8 Register Description

Offset	0x20			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_gpioie_0_reg	WR	0x0	• 1: Unmask • 0: Mask
[4:31]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG IOIRQ 9

Table 2-762 AON IOMUX CFGSAIF SYSCFG IOIRQ 9 Register Description

Offset	0x24			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_gpioris_0_reg	RO	0x0	Status of the edge trigger,can be cleared by writing gpioic
[4:31]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG IOIRQ 10

Table 2-763 AON IOMUX CFGSAIF SYSCFG IOIRQ 10 Register Description

Offset	0x28			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_gpiomis_0_reg	RO	0x0	The masked GPIO IRQ status
[4:31]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG IOIRQ 11

Table 2-764 AON IOMUX CFGSAIF SYSCFG IOIRQ 11 Register Description

Offset	0x2c			
Default	0x0			
Bit	Name	Access	Default	Description
[0:3]	aon_gpio_in_sync2_0_reg	RO	0x0	Status of gpio_in after synchroniza-tion
[4:31]	Reserved	None	0x0	Reserved

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AON IOMUX CFG SAIF SYSCFG 48

Table 2-765 AON IOMUX CFG SAIF SYSCFG 48 Register Description

Offset	0x30			
Default	0x0			
Bit	Name	Access	Default	Description
[0]	PADCFG_PAD_TESTEN_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[1:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 52

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-766 AON IOMUX CFG SAIF SYSCFG 52 Register Description

Offset	0x34			
Default	0x1			
Bit	Name	Access	Default	Description
[0]	PADCFG_PAD_RGPIO0_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_RGPIO0_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_RGPIO0_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_RGPIO0_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_RGPIO0_SLEW	WR	0x0	Slew Rate Control:

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Table 2-766 AON IOMUX CFG SAIF SYSCFG 52 Register Description (continued)

Offset	0x34			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
				• 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_RGPIO0_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_RGPIO0_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 56

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-767 AON IOMUX CFG SAIF SYSCFG 56 Register Description

Offset	0x38			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_RGPIO1_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_RGPIO1_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_RGPIO1_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_RGPIO1_PD	WR	0x0	*Pull-Down (PD)* settings:

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Table 2-767 AON IOMUX CFG SAIF SYSCFG 56 Register Description (continued)

Offset	0x38			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
				• 1: Yes • 0: No
[5]	PADCFG_PAD_RGPIO1_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_RGPIO1_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_RGPIO1_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 60

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-768 AON IOMUX CFG SAIF SYSCFG 60 Register Description

Offset	0x3c			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_RGPIO2_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_RGPIO2_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_RGPIO2_PU	WR	0x0	*Pull-Up (PU)* settings:

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Table 2-768 AON IOMUX CFG SAIF SYSCFG 60 Register Description (continued)

Offset	0x3c			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
				• 1: Yes • 0: No
[4]	PADCFG_PAD_RGPIO2_PD	WR	0x0	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_RGPIO2_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_RGPIO2_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_RGPIO2_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 64

The register can be used to configure the core settings of system signals. The signal name is indicated in the "Name" column of the following table per StarFive naming conventions. For example, "PADCFG_PAD_GPIO0_IE" indicates the attribute "IE" of the signal "GPIO0". See Signal Description *(on page 62)* for a complete list of the system signals.

Table 2-769 AON IOMUX CFG SAIF SYSCFG 64 Register Description

Offset	0x40			
Default	**0x11**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_RGPIO3_IE	WR	0x1	*Input Enable (IE)* Controller: • 1: Enable the receiver • 0: Disable the receiver
[1:2]	PADCFG_PAD_RGPIO3_DS	WR	0x0	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA.

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Table 2-769 AON IOMUX CFG SAIF SYSCFG 64 Register Description (continued)

Offset	0x40			
Default	**0x11**			
Bit	**Name**	**Access**	**Default**	**Description**
				• 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[3]	PADCFG_PAD_RGPIO3_PU	WR	0x0	*Pull-Up (PU)* settings: • 1: Yes • 0: No
[4]	PADCFG_PAD_RGPIO3_PD	WR	0x1	*Pull-Down (PD)* settings: • 1: Yes • 0: No
[5]	PADCFG_PAD_RGPIO3_SLEW	WR	0x0	Slew Rate Control: • 0: Slow (Half frequency) • 1: Fast
[6]	PADCFG_PAD_RGPIO3_SMT	WR	0x0	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[7]	PADCFG_PAD_RGPIO3_POS	WR	0x0	*Power-on-Start (POS)* enabler: • 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[8:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 68

Table 2-770 AON IOMUX CFG SAIF SYSCFG 68 Register Description

Offset	0x44			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
[0]	PADCFG_PAD_RSTN_SMT	WR	0x1	*Active high Schmitt (SMT)* trigger selector: • 0: No hysteresis • 1: Schmitt trigger enabled
[1]	PADCFG_PAD_RSTN_POS	WR	0x0	*Power-on-Start (POS)* enabler:

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Table 2-770 AON IOMUX CFG SAIF SYSCFG 68 Register Description (continued)

Offset	0x44			
Default	**0x1**			
Bit	**Name**	**Access**	**Default**	**Description**
				• 1: Enable active pull down for loss of core power • 0: Active pull-down capability disabled
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 76

Table 2-771 AON IOMUX CFG SAIF SYSCFG 76 Register Description

Offset	0x4c			
Default	**0x2**			
Bit	**Name**	**Access**	**Default**	**Description**
[1:0]	PADCFG_PAD_RTC_DS	WR	0x2	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 84

Table 2-772 AON IOMUX CFG SAIF SYSCFG 84 Register Description

Offset	0x54			
Default	**0x2**			
Bit	**Name**	**Access**	**Default**	**Description**
[1:0]	PADCFG_PAD_OSC_DS	WR	0x2	Output *Drive Strength (DS)*: • 00: The rated drive strength is 2 mA. • 01: The rated drive strength is 4 mA. • 10: The rated drive strength is 8 mA. • 01: The rated drive strength is 12 mA.
[2:31]	Reserved	None	0x0	Reserved

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AON IOMUX CFG SAIF SYSCFG 88

Table 2-773 AON IOMUX CFG SAIF SYSCFG 88 Register Description

Offset	0x58			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_MDC_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 92

Table 2-774 AON IOMUX CFG SAIF SYSCFG 92 Register Description

Offset	0x5c			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_MDIO_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 96

Table 2-775 AON IOMUX CFG SAIF SYSCFG 96 Register Description

Offset	0x60			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_RXD0_-syscon	WR	0x2	• [1:0] = 0 : GMAC0 IO voltage select 3.3 V • [1:0] = 1: GMAC0 IO voltage select 2.5 V • [1:0] = 2: GMAC0 IO voltage select 1.8 V
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 100

Table 2-776 AON IOMUX CFG SAIF SYSCFG 100 Register Description

Offset	0x64			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_RXD1_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

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AON IOMUX CFG SAIF SYSCFG 104

Table 2-777 AON IOMUX CFG SAIF SYSCFG 104 Register Description

Offset	0x68			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_RXD2_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 108

Table 2-778 AON IOMUX CFG SAIF SYSCFG 108 Register Description

Offset	0x6c			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_RXD3_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 112

Table 2-779 AON IOMUX CFG SAIF SYSCFG 112 Register Description

Offset	0x70			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_RXDV_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 116

Table 2-780 AON IOMUX CFG SAIF SYSCFG 116 Register Description

Offset	0x74			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_RXC_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

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AON IOMUX CFG SAIF SYSCFG 120

Table 2-781 AON IOMUX CFG SAIF SYSCFG 120 Register Description

Offset	0x78			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_TXD0_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 124

Table 2-782 AON IOMUX CFG SAIF SYSCFG 124 Register Description

Offset	0x7c			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_TXD1_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 128

Table 2-783 AON IOMUX CFG SAIF SYSCFG 128 Register Description

Offset	0x80			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_TXD2_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 132

Table 2-784 AON IOMUX CFG SAIF SYSCFG 132 Register Description

Offset	0x84			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_TXD3_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

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AON IOMUX CFG SAIF SYSCFG 136

Table 2-785 AON IOMUX CFG SAIF SYSCFG 136 Register Description

Offset	0x88			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_TXEN_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFG SAIF SYSCFG 140

Table 2-786 AON IOMUX CFG SAIF SYSCFG 140 Register Description

Offset	0x8c			
Default	0x2			
Bit	Name	Access	Default	Description
[1:0]	PADCFG_PAD_GMAC0_TXC_syscon	WR	0x2	
[2:31]	Reserved	None	0x0	Reserved

AON IOMUX CFGSAIF SYSCFG 144

Table 2-787 AON IOMUX CFGSAIF SYSCFG 144 Register Description

Offset	0x90			
Default	0x0			
Bit	Name	Access	Default	Description
[1:0]	PAD_GMAC0_RXC_func_sel	WR	0x0	Function selector of GMAC0_RXC: • Function 0: u0_aon_crg.clk_gmac0_-rgmii_rx • Function 1: u0_aon_crg.clk_gmac0_rmi-i_ref • Function 2: None • Function 3: None
[2:31]	Reserved	None	0x0	Reserved

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3. Power Management

This section describes power mode, power management, and peripheral power management.

3.1. Overview

The system includes 10 hierarchies with the prefix of “dom”. Each hierarchy represents an independent power domain. All analog PHY are positioned on the top layer.

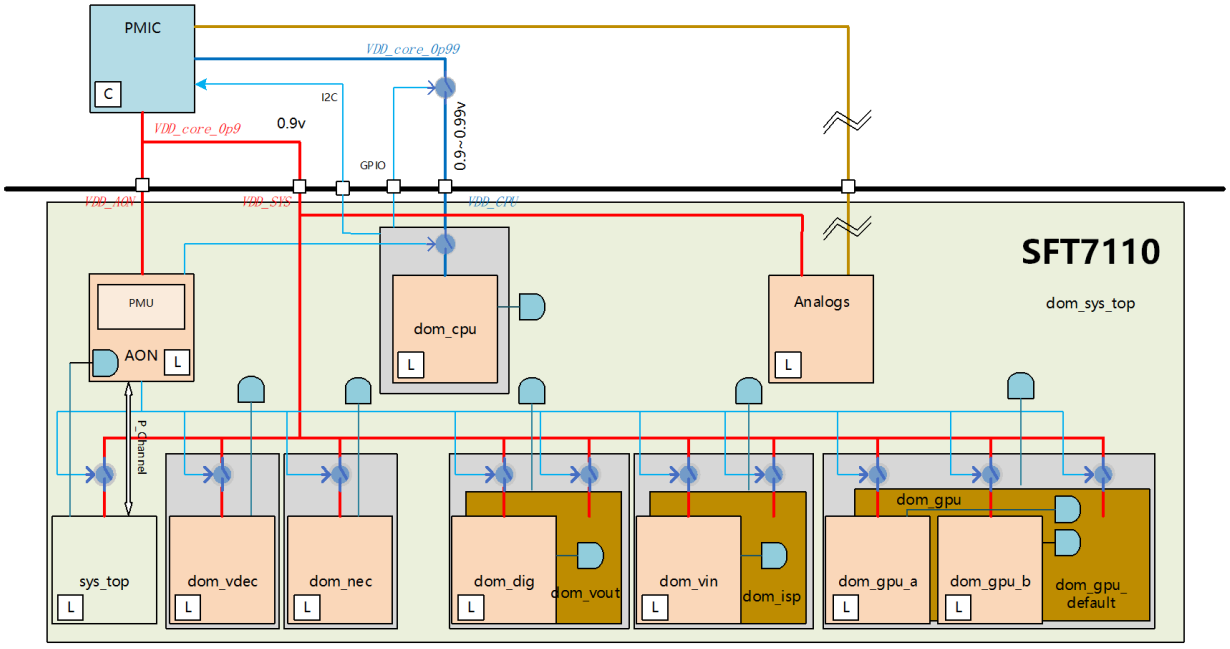
In the 10 power domains, **dom_aon** is a “always-on” power domain. It is used for waking up from sleep. The supported modules include:

- Real Time Clock (RTC)
- General Purpose Input and Output (GPIO)
- Wake-on-LAN (WoL)

The GPU of JH-7110 contains the following 3 power domains.

1. **dom_gpu_default**: Share the same control with the top layer.
2. **dom_gpu_a**: Share the same control with the top layer.
3. **dom_gpu_b**: An independent power domain which enables software power-on and power-off.

Figure 3-1 Power Structure Block Diagram



LP Cell Placement Architecture

The following list provides the architecture details:

- Overview
  - Feeds power from external PMIC
  - Includes 3 power groups: Vdd_core_0v9, Vdd_core_0v99, and Vdd_ana
  - Vdd_core_0v99 can be switched off on board level
- Power domain

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    - Includes 8 power domains
    - *Always-On (AON)* domains are the always on modules for the entire SoC.
    - The dom_cpu module is for Vdd_core_0p99, and all the other modules are for Vdd_core_0p9;
    - The dom_isp, dom_vout, and dom_gpu modules contain 2-3 power domains each, while the other modules only contain 1.
- Power switch: The power switch of each independent PR is controlled by the UPF, which is placed in the module itself. The EN control signal comes from the input port of the module.
- Isolation:
    - The isolation of module-to-module signals are controlled by top-layer UPF, Which is placed in the dom_sys_top module of the SoC top, and fed power by Vdd_core_0v9
    - The 3 modules of dom_isp, dom_vout, and dom_gpu contains 2-3 power domains. The isolation of the intra-module signals are controlled by the UPF of the module, which is placed on the top layer of the module and fed power by Vdd_core_0v9
- Level shifter:
    - The dom_cpu output signal + high-to-low cell, place is dom_sys_top
    - The dom_cpu input signal + low-to-high cell, place is dom_cpu_top
    - For the signal overlap between Level l and ISO, select Level 1 cell with EN

3.2. Analog PHY Power

3.2.1. DDR PHY

The DDR PHY of JH-7110 has the following analog power characteristics.

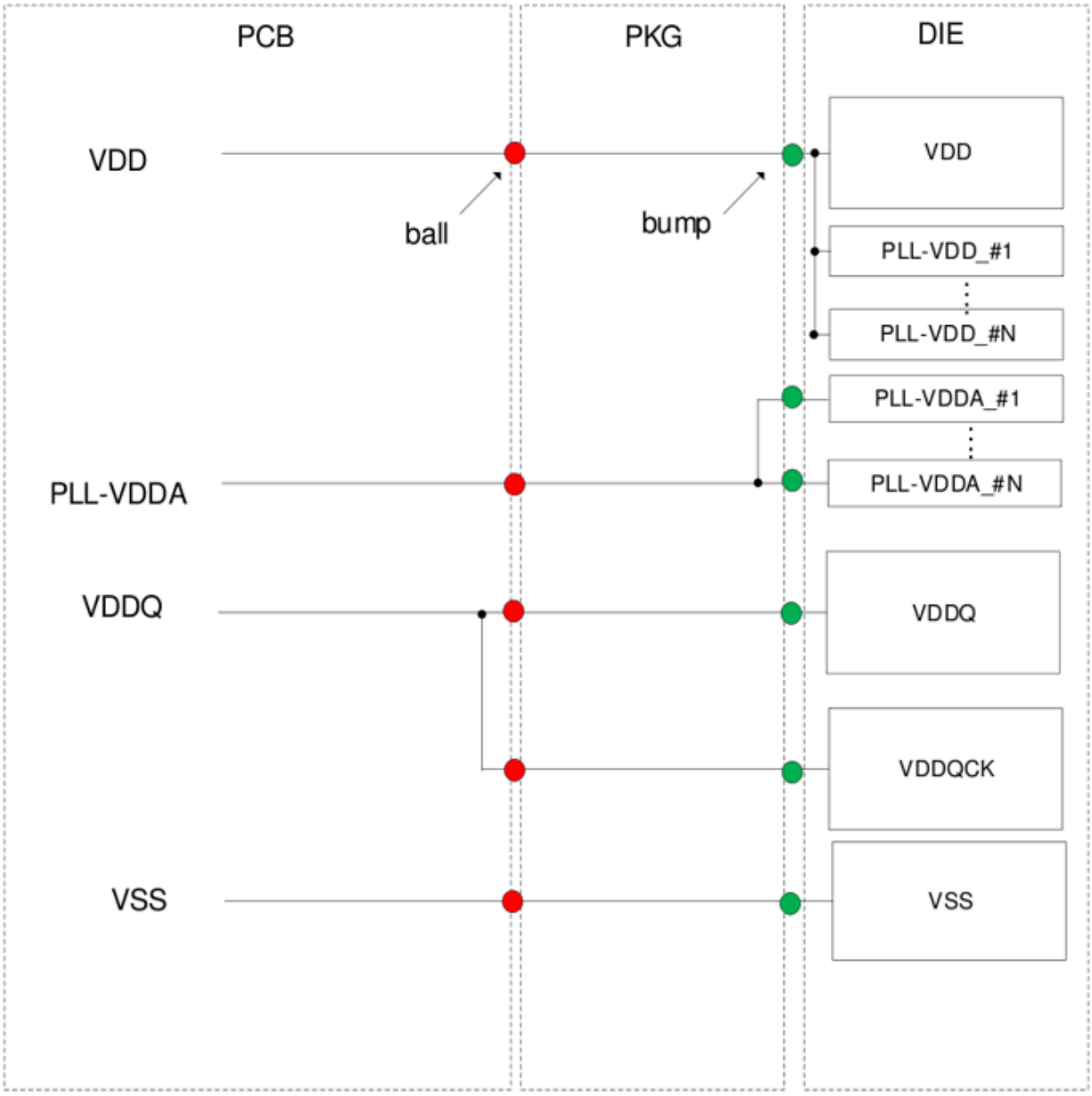
- All power outputs are generated from bump.
- PHY switch off the power supply only in sleep mode.
- Before entering the sleep mode, CPU will turn off the PHY power supply via board level switch.

Note the following for DDR PHY power integration.

- The SoC VSS can be short with PHY VSS in die by connecting the SoC and PHY VSS bump together using AP RDL layer.
- PHY VDD cannot be short with SoC VDD in die.
- You can short the PHY VDD with SoC VDD at package or PCB level as long as VDD noise target is met.

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Figure 3-2 DDR PHY Power Diagram



3.2.2. MIPI RX

The MIPI receiver of JH-7110 has the following analog power characteristics.

- VCC09D is a independent pad output.
- VCC18A/VCC09A generates output from the system pad.
- VCC18A/VCC09A and VCC09D are controlled on the board level.

Power and Ground

The following table provides the power and ground information.

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Table 3-1 MIPI RX Analog and Digital Power Supplies

Name	Value	Description
VCC09A	0.9V (-5% + 10% with respect to GNDA)	0.9 V analog supply with pad.
VCC09D	0.9V (±10% with respect to GND09D)	0.9 V digital supply.
VCC18A	1.8V (±10% with respect to GNDA)	1.8 V analog supply with pad.

The analog power supplies should be isolated from the power supplies of the ASIC to prevent extra jitter caused by the unexpected noise. As to the VCC09D andGND09D, it is permitted to share with the core power of the ASIC. In addition, the power/ground connection should provide a robust and low-impedance plane for ESD protection.

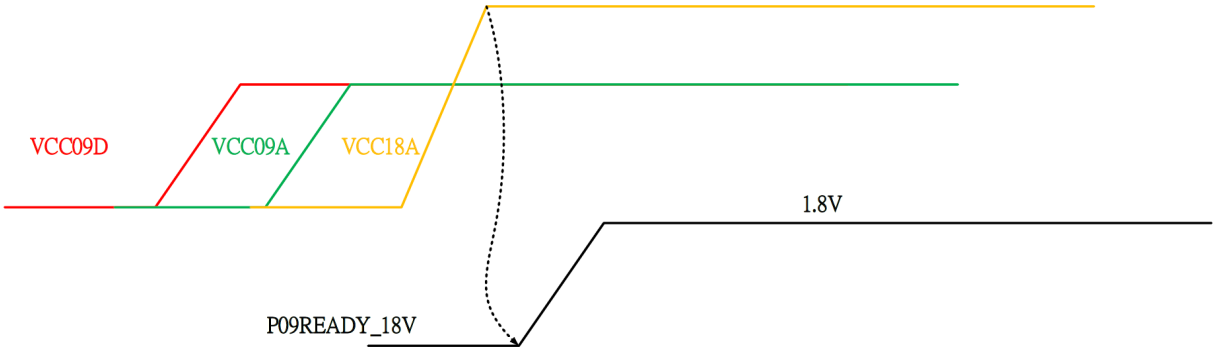
Table 3-2 MIPI RX Analog Pad and Power/Ground

Pin Name	Direction	With PAD	Description
VCC09D	Input	No	0.9 V digital supply voltage that connects to the core power.
GND09D	Input	No	Digital ground supply that connects to the core power.
VCC09A	Input	Yes	0.9 V analog supply voltage. 1uF external capacitor is needed.
VCC18A	Input	Yes	1.8 V analog supply voltage. 1uF external capacitor is needed.
GNDA	Input	Yes	Analog ground supply for the analog part.

Power On Requirements

There are 3power domains in this IP, VCC09A, VCC18A and VCC09D. The VCC09A and VCC09D are 0.9 V while VCC18A is 1.8 V typically. The recommended sequence is to power up the VCC09D first. The signal P09READY_18V should be 0 - 1.8 V after the powers are ready.

Figure 3-3 MIPI RX Power On Sequence



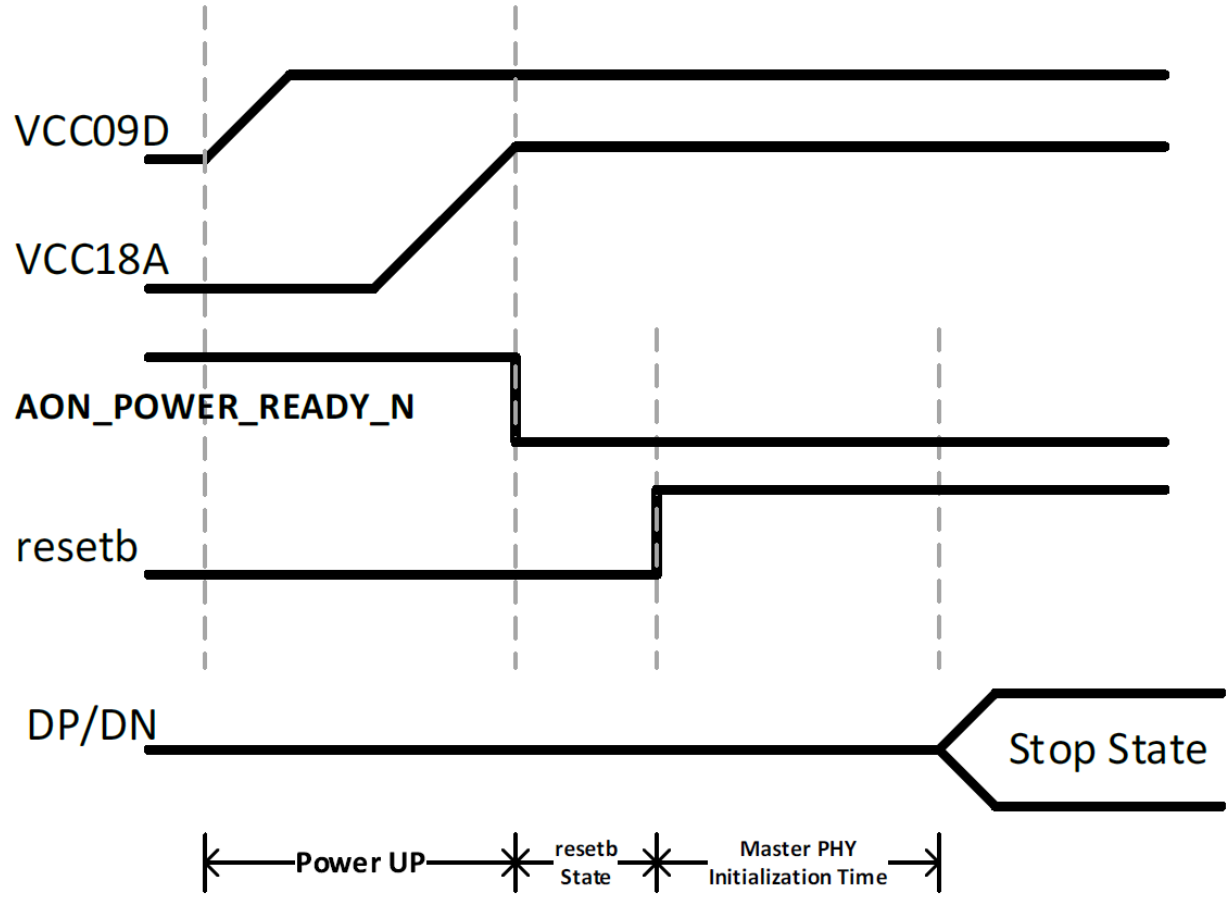
3.2.3. MIPI TX

The MIPI transceiver of JH-7110 has the following analog power characteristics.

- VCC09D and VCC18A are independent pad outputs.
- VCC18A and VCC09D are controlled on the board level.

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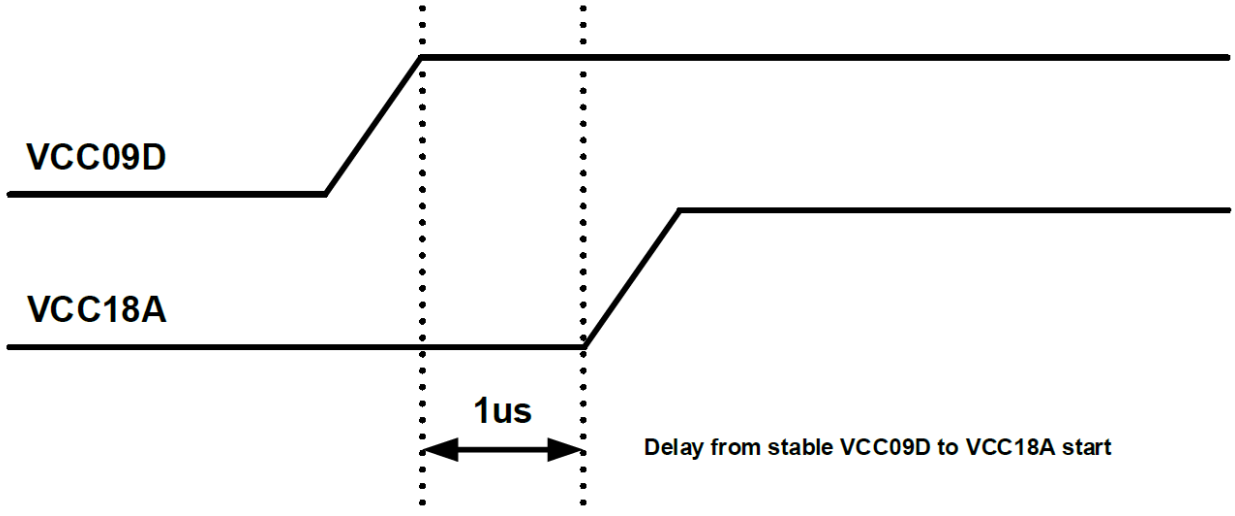
Figure 3-4 MIPI TX Power Up Timing



The recommended power up sequence is that from digital core voltage to analog I/O voltage and from low voltage level to high voltage level. This is not considered as a constraint, but a guideline instead, as it results in the best-case operating scenario, where the leakage currents during powering up are kept to a minimum.

For keeping leakage current during power up to a minimum, the powering up sequence guideline would be from digital core voltage to analog I/O voltage and from low voltage level to high voltage level. There are 2 power domains in M31DPHYTX512TL028D, which are VCC09D and VCC18A. The VCC09D is 0.9V supplies, and VCC18A is 1.8V. So, the recommended powering up sequence for this IP is to power up VCC09D first, and then power up VCC18A at the following.

Figure 3-5 MIPI TX Power Up Sequence



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Table 3-3 MIPI TX Analog Pad and Power/Ground

Pin Name	Direction	With PAD	Description
VCC09D	Input	No	0.9V digital supply voltage that connects to the core power.
GND09D	Input	No	Digital ground supply that connects to the core power.
VCC18A	Input	Yes	1.8V analog supply voltage for the DPHY analog part.

3.2.4. OTP

The OTP of JH-7110 has the following analog power characteristics.

- VDD and sys_top has the same power characteristics.
- VDD2 generates output from the pad.

Figure 3-6 OTP Power Characteristics

DC Specifications (T_J= -40℃ to 125℃)

Recommended DC Operating Conditions

Operating Mode	Power Pin	Min	Typ	Max	Unit
Read Mode	V_{DD}	0.81	0.9	0.99	V
	V_{DD2}	1.62	1.8	1.98	V
	V_{SS}		0		
PGM Mode	V_{DD}	0.81	0.9	0.99	V
	V_{DD2}	1.62	1.8	1.98	V
	V_{SS}		0		

[7.566] © eMemory EG512X32TH028CW01

Notes

1. **Power supply voltage beyond DC operating range is not guaranteed.**
2. **Power/Ground bouncing beyond DC operating range might cause invalid data output. It's not guaranteed by eMemory and customers must take care of power stability on their own.**
3. **Normally, operating junction temperature is from -40℃ to 125℃, and Program operation should be at junction temperature -40℃ ~ 125℃.**

3.2.5. PCIE

The PCIE Multi-Purpose PHY of JH-7110 has the following analog power characteristics.

- Provide AVDH/AVDL pad output
- Independent VDD pad output
- Controlled on the board level.

Power Up Sequence

The PHY has three power supplies, VDD, AVDL and AVDH. VDD and AVDL are both Core Power supplies and while separate pins are used for noise isolation purposes. AVDH is the IO Power supply.

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Figure 3-7 PCIE Power-Up Sequence 1 (AVDH→AVDL→VDD or AVDH→VDD→AVDL)

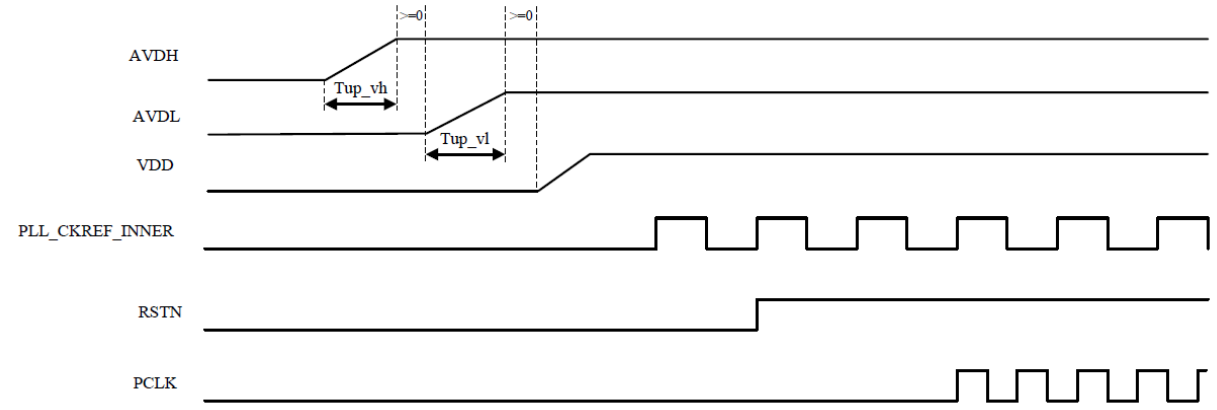


Figure 3-8 PCIE Power-Up Sequence 2(VDD→AVDL→AVDH or AVDL→VDD→AVDH)

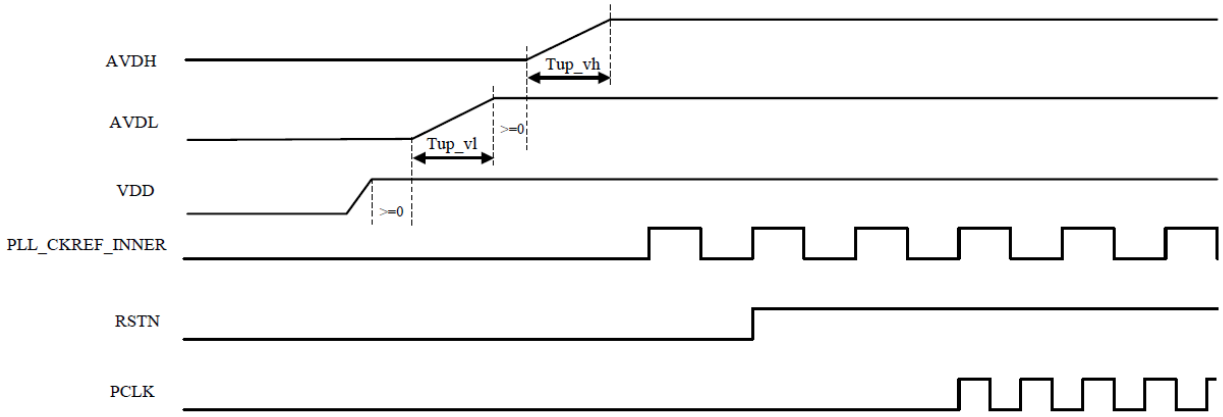


Table 3-4 PCIE Power-on Time Information

Symbol	Parameter	Min	Typ	Max	Unit
Tup_vh	The power-on time of AVDH	0.3			ms
Tup_vl	The power-on time of AVDL	0.5			ms

Note:
If the power-on time of AVDL or AVDH is too short, there may be large pulse current during the power on process, the maximum of pulse current may be greater than 400mA when the power-on time is 100us.

Power Down Sequence

The PHY has three power supplies,VDD, AVDL and AVDH.VDD and AVDL are both Core Power supplies and while separate pins are used for noise isolation purposes. AVDH is the IO Power supply.

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Figure 3-9 PCIE Power Down Sequence

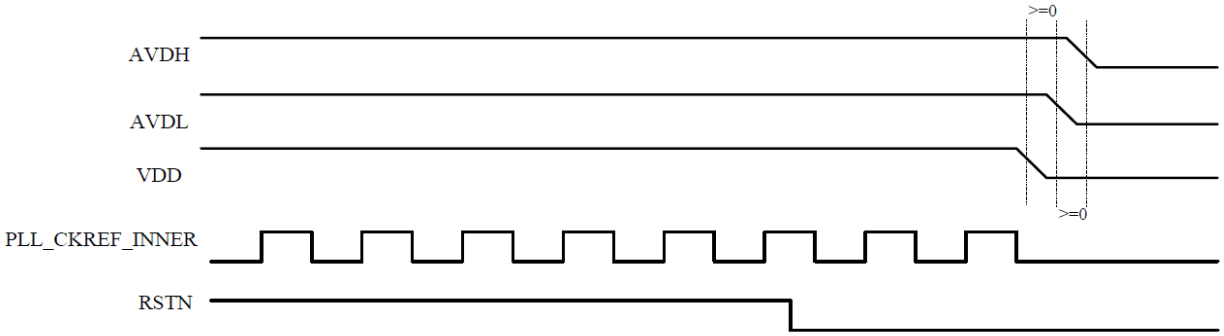


Table 3-5 PCIE IO PAD

Group	Name	Dir	#	Description
Analog P/G	AVDH	PAD	*	1.8Vanalog power supply
	AVDL	PAD	*	0.9Vanalog power supply
	AVSS	PAD	*	analog ground
High Speed signal	RXP	PAD	1	differential data input of RX, positive
	RXN	PAD	1	differential data input of RX, negative
	TXP	PAD	1	differential data output of TX, positive
	TXN	PAD	1	differential data output of TX, negative
Reference Clock input/output	CKREFP	PAD	1	Differential pair that can be configured as either a reference clock input or a reference clock output. CKREF_SRC[1:0]=01: CKREFP/N are used as input reference clock source CKREF_SRC[1:0]=10: CKREFP/N are used as output clock to supply a differential 100M reference clock. See Table 3-6 : PCIE Reference Clock Input/Output *(on page 491)* for more information. **Note:** CKREFP/N is valid means CKREFP/N can output 100MHz differential clock.
	CKREFN	PAD	1	
Digital P/G	VDD/VDDA/VDDB	PIN		VDD/VSS –Digital Power from core side.
	VSS/VSSA/VSSB	PIN		VDDA/VDDB/VSSA/VSSB –PIN of Power Cut IO between Analog Power Domain and Digital Power Domain

Table 3-6 PCIE Reference Clock Input/Output

CKREF_SRC[1:0]	CLKREQ	L1SUB_ENTREQ	PWDN[1:0]	CKREFP/N
Input				**Output**
10	1	X	X	Valid

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Table 3-6 PCIE Reference Clock Input/Output (continued)

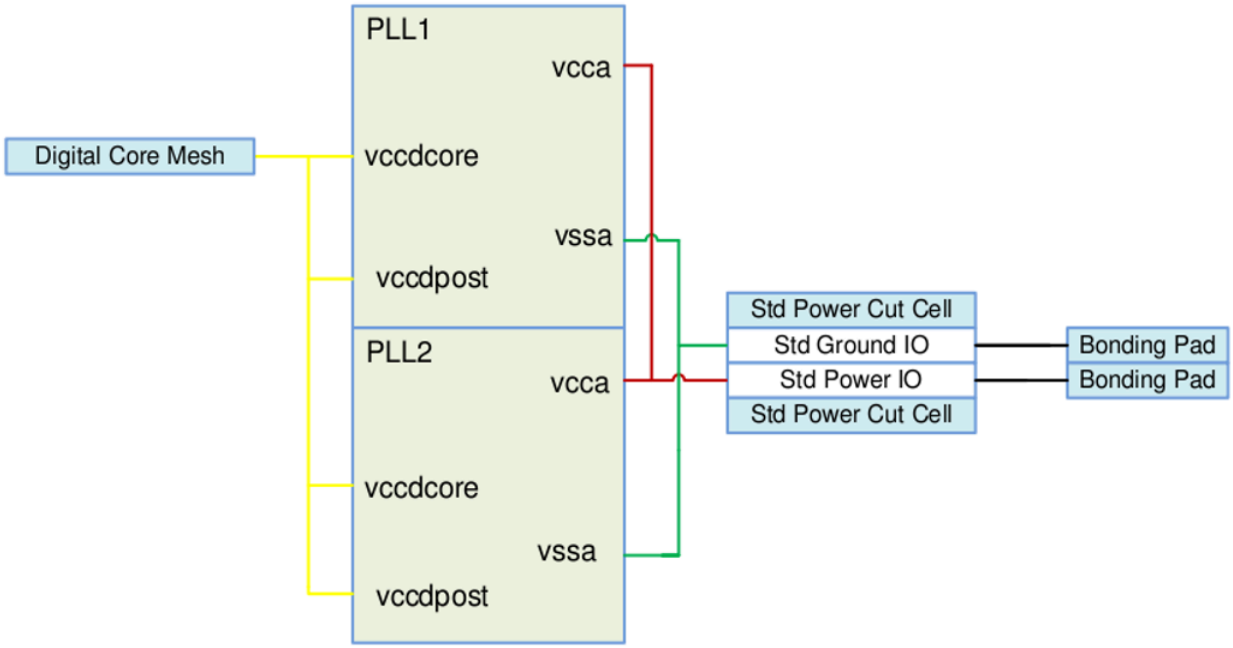
CKREF_SRC[1:0]	CLKREQ	L1SUB_ENTREQ	PWDN[1:0]	CKREFP/N
Input				**Output**
10	0	1	X	Not valid
10	0	0	00/01/10	Valid
10	0	0	11	Not valid

3.2.6. PLL

The PLL of JH-7110 has the following analog power characteristics.

- VDD connects to sys_top
- VCCA pad output

Figure 3-10 PLL PAD Placement Example



3.2.7. Temperature Sensor

The Temperature Sensor of JH-7110 has the following analog power characteristics.

- VDD connects to sys_top
- VCCA pad output

Table 3-7 Temperature Sensor Power Pin Information

Pin	Description	Type	Comment
VDD	Digital supply	Power	Usually connected to the ASIC digital core supply.
VDDA	Analog supply	Power	Usually connected to the a dedicated analog supply pin.
VSS	Ground	Ground	Combined ground.

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3.2.8. USB

The USB of JH-7110 has the following analog power characteristics.

- VDDA connects to sys_top
- VCCA18/VCCA33 generates output from pad, and supports board level switch control

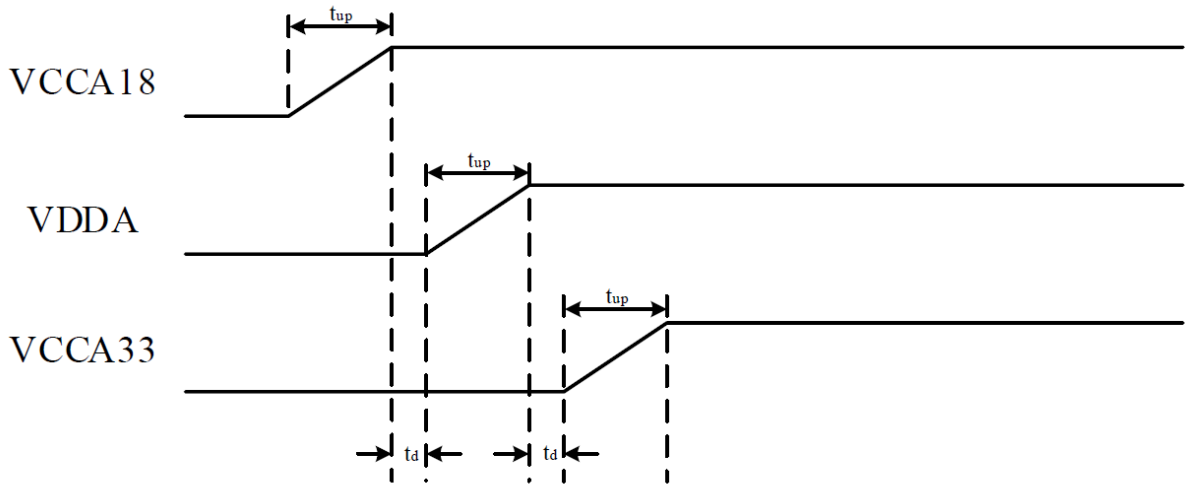
Table 3-8 USB ASIC Transceiver Analog IO PAD Signals

Name	Dir	Description
VCCA33	P	3.3V power supply(only Full speed driver)
VCCA18	P	1.8V power supply
VDDA	P	0.9V power supply
AGND	G	Ground IO for both 3.3V,1.8V and 0.9V

Power Up Sequence

There are three powers and they are VCCA33(3.3V)、VCCA18(1.8V) and VDDA(0.9V), IP supports power up sequence in any combination because it has power-off protection design between the three powers. But there is a over voltage case that 1.8V MOSFET works under 3.3V power, the IP has breakdown voltage design to protect the 1.8V MOSFET, but anyway we suggest to power up VCCA33(3.3V) finally for protecting the 1.8V MOSFET during the power-on period.

Figure 3-11 USB Power Up Sequence 1



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Figure 3-12 USB Power Up Sequence 2

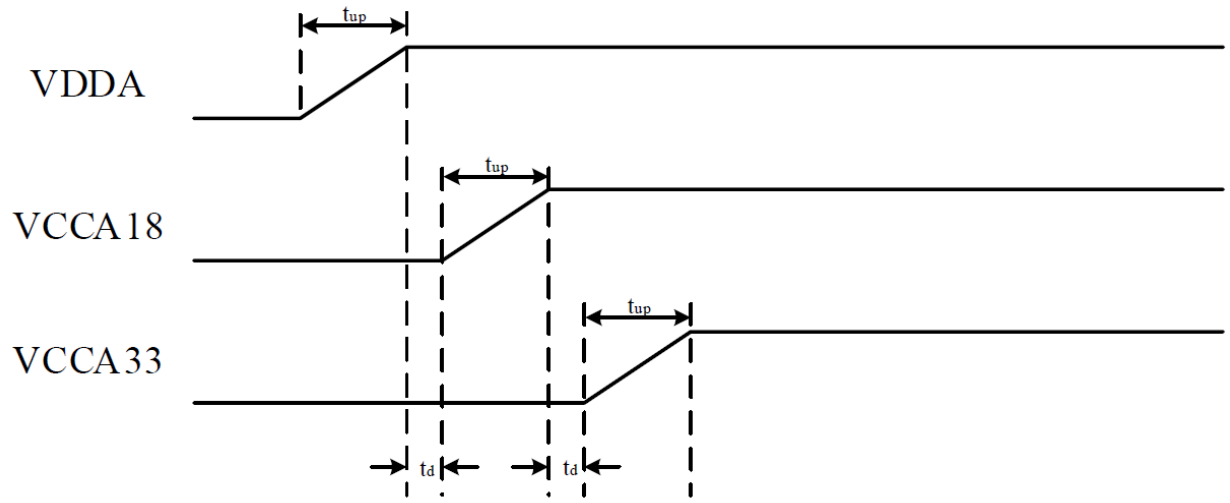


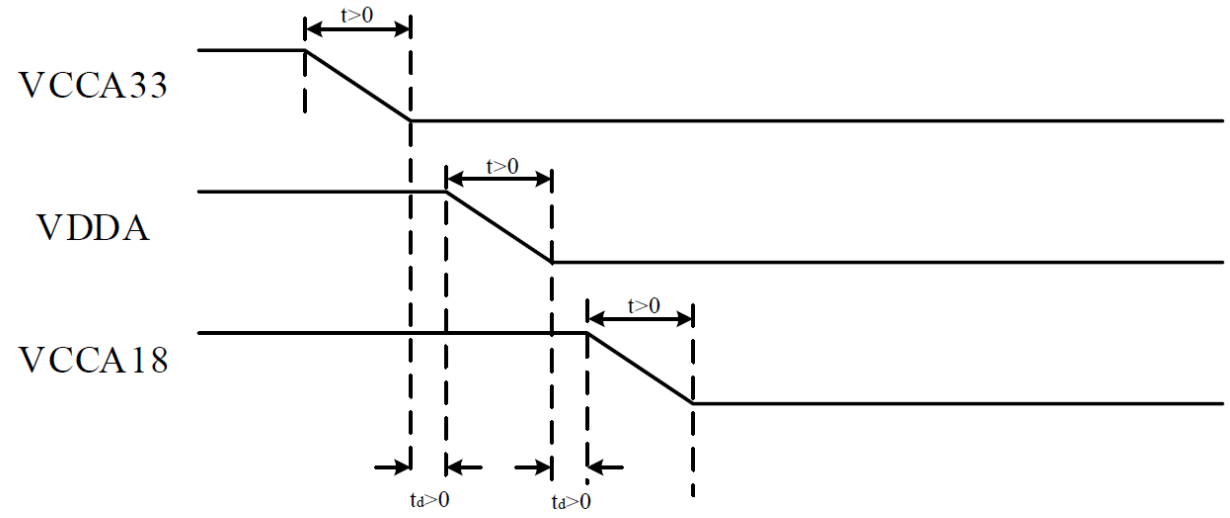
Table 3-9 USB Power Up Parameter

Name	Description	Min	Typ	Max	Unit
t_{up}	the time of power-up	200			us
t_d	the delay of two power-up	>0			us

Power Down Sequence

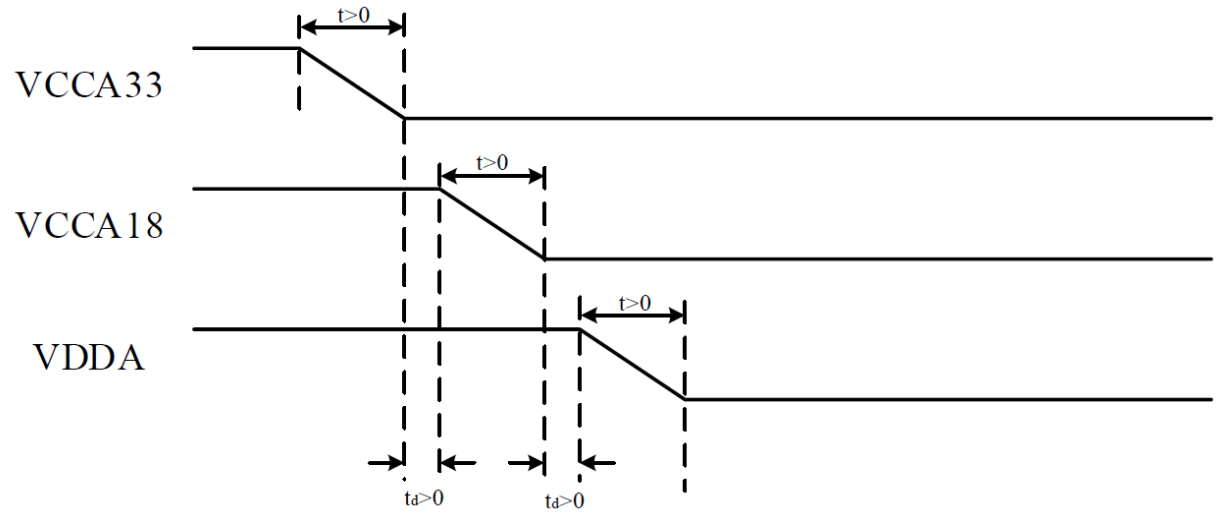
There are three powers and they are VCCA33(3.3V)、VCCA18(1.8V) and VDDA(0.9V), IP supports power up sequence in any combination because it has power-off protection design between the three powers. But there is a over voltage case that 1.8V MOSFET works under 3.3V power, the IP has breakdown voltage design to protect the 1.8V MOSFET, but anyway we suggest to power down VCCA33(3.3V) first for protecting the 1.8V MOSFET during the power-on period.

Figure 3-13 USB Power Down Sequence 1



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Figure 3-14 USB Power Down Sequence 2



3.3. Power Modes

In the following power mode table, GPU is split into Power Domain A and Power Domain B. The entire GPU including Power Domain A and Power Domain B can be powered on and off by software. When Power Domain A is on, Power Domain B can be controlled by MIPS core in Domain A, so called Active Power Management.

Note:
Make sure you know that GPU does not support DFVS.

Figure 3-15 Power Modes

PD / mode	AON	dom0(top)	dom1(cpu)(hv)	dom2(gpu_a)	dom3(vdec)	dom4(vout)	dom5(isp)	dom6(venc)	dom7(gpu_b)
Normal	Y	Y	Y	Y	Y	Y	Y	Y	Y
Rest1	Y	Y	Y	SW	SW	SW	SW	SW	SW
Rest2	Y	Y	N	SW	SW	SW	SW	SW	SW
Sleep	Y	N	N	N	N	N	N	N	N

3.4. Power Supply

3.4.1. Power-Up Sequence

JH-7110 has 3 power supplies, VDD, AVDL, and AVDH. VDD and AVDL are both core power supplies and while separate pins are used for noise isolation purposes.

The recommended power sequence is that from digital core voltage to analog I/O voltage and from low voltage level to high voltage level. This is not considered a constraint, but instead, a guideline, as it could result in the best-case operating scenario, where the leakage currents during power up are kept to a minimum.

The following diagram shows the recommended power-on sequence of different power groups.

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Figure 3-16 Power Up Sequence

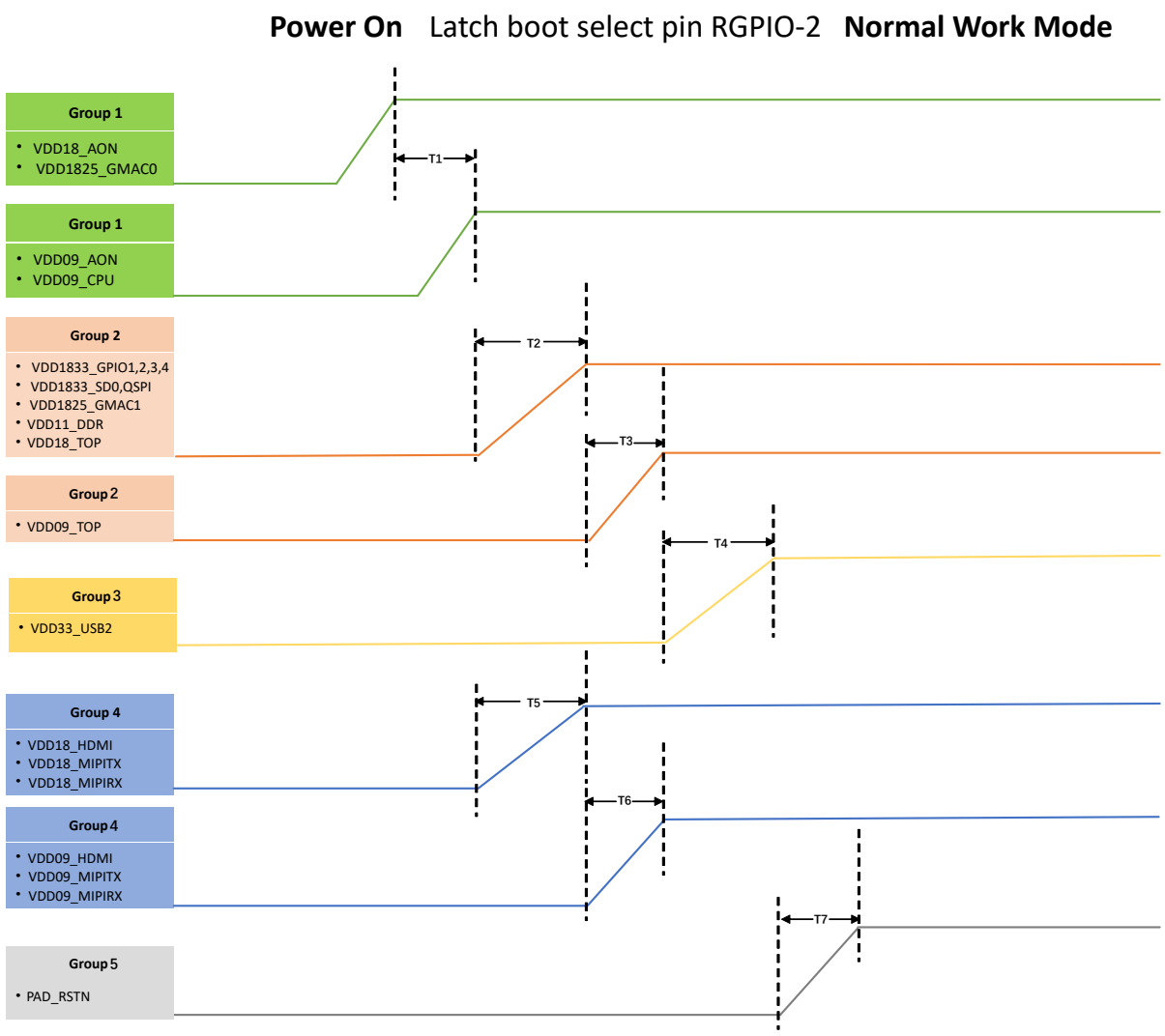


Table 3-10 Power Up Sequence Intervals

Sequence	Interval
T1	100 us
T2	300-500 us
T3	50-100 us
T4	300-500 us
T5	300-500 us
T6	50-100 us
T7	>10 ms

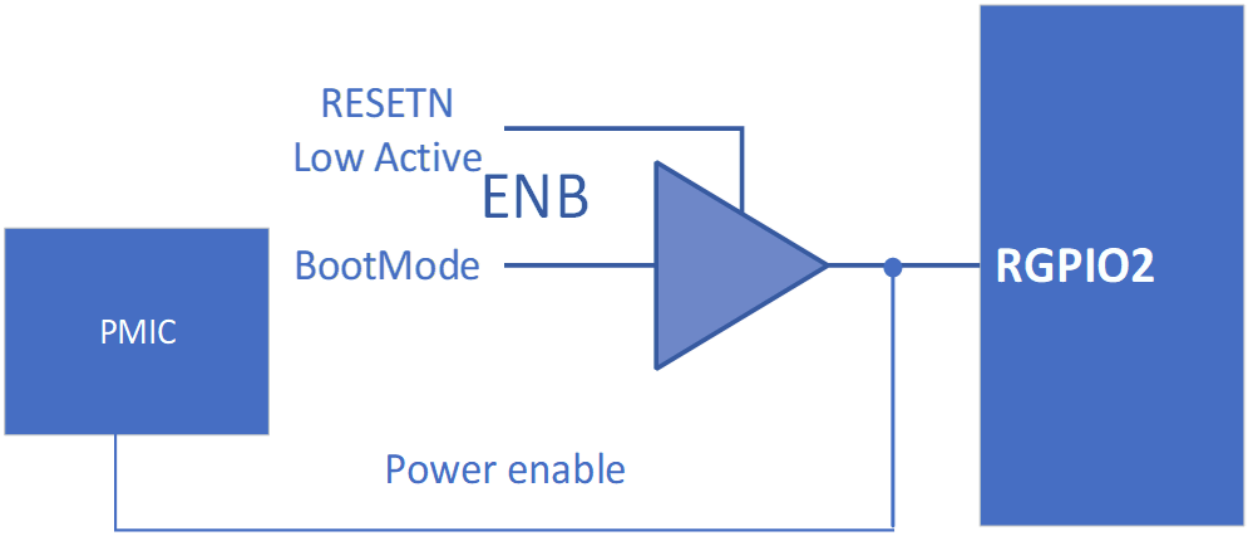
3.4.2. Standby and Wakeup

Block Diagram

The following figure shows the standby and wakeup block diagram.

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Figure 3-17 Standby and Wakeup Block Diagram



Entering Standby Mode

To enter standby mode, only Always-On (AON) *(on page 555)* modules should be working, including PMU, RTC, and GMAC.

1. CPU controls PMIC via I2C, with VDD18_HDMI, MIPITX, and MIPIRX powered off.
2. CPU controls PMIC or the power switches in MIPITX and RX via I2C, with DD09_MIPITX and MIPIRX powered off, to which either internal or external power supplies can be connected. When internal power supplies are fed, the 2 pins can be switched on and off independently.
3. CPU switches off all digital IP except for CPU itself and SYSTOP by configuring PMU power-down sequence.
4. To configure standby wakeup source registers, the following three wakeup methods are supported: Wake up via RTC, via GMAC0, and via GPIO3.
5. When the CPU switches off itself and SYSTOP by configuring the PMU power-down sequence, PMU could drag down or close the TOP power supplies (Orange pins in the figure: Figure 3-16 : Power Up Sequence *(on page 496)*) via GPIO2.

Waking Up from Standby Mode

To wake up from standby mode:

1. Wakeup via RTC: RTC automatically switches on CPU, SYSTOP, and the TOP power supplies (Orange pins in the figure: Figure 3-16 : Power Up Sequence *(on page 496)*) by dragging up GPIO2. System will follow requirements to switch on other power supplies.

   Note:

   - The control signal from GPIO2 to PMIC is active only when RESETN is high, otherwise, the signal is de-activated.
   - Use PMU to control the ON/OFF of the PMIC, a low-EN 3-state switch can be added.

2. Wakeup via Remote Ethernet: The remote GMAC0 sends interrupts to PMU to wake up CPU, SYSTOP, and the TOP power supplies (Orange pins in the figure: Figure 3-16 : Power Up Sequence *(on page 496)*) by dragging up GPIO2. System will follow requirements to switch on other power supplies.
3. Wakeup via GPIO: Press the button to initiate high-level pulses via GPIO3, and trigger PMU to wake up CPU, SYSTOP, and the TOP power supplies (Orange pins in the figure: Figure 3-16 : Power Up Sequence *(on page 496)*) by dragging up GPIO2. System will follow requirements to switch on other power supplies.

3.4.3. Power Group Description

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Table 3-11 Power Group Description

Group	Name	Dir	Description
Analog P/G	AVDH	PAD	1.8 V analog power supply
	AVDL	PAD	0.9 V analog power supply
	AVSS	PAD	Analog ground
High-Speed Signal	RXP	PAD	Differential data input of RX, positive
	RXN	PAD	Differential data input of RX, negative
	TXP	PAD	Differential data output of TX, positive
	TXN	PAD	Differential data output of TX, negative
Reference Clock Input/Output	CKREFP	PAD	Differential pair that can be configured as either a reference clock input or a reference clock output, P for positive and N for negative.
	CKREFN	PAD	
Digital P/G	VDD/VDDA/VDDB	PIN	VDD/VSS – Digital Power from the core inside. VDDA/VDDB/VSSA/VSSB – PIN of Power Cut IO between Analog Power Domain and Digital Power Domain.
	VSS/VSSA/VSSB	PIN	

3.5. Power Mode

Power modes include normal run mode with the Power Dial option and wait-for-interrupt clock gating mode using the WFI instruction. Additionally, there is a full power down mode supported via the CEASE instruction.

Run Mode

In run mode, the hart is fully operational, and we also provide the option to include coarse-grained architectural clock gating.

WFI Clock Gate Mode

WFI clock gating mode can be entered by executing the WFI instruction.

3.6. PMU

3.6.1. Overview

In order to meet low power requirements, a *Power Management Unit (PMU)* is designed for controlling power resources in JH-7110.

PMU manages the power mode switching of JH-7110. It accepts software and hardware encourage to switch power mode of JH-7110.

3.6.2. Feature

The PMU of JH-7110 has the following features.

- Support APB Interface
- Support software encouragement
- Support hardware encouragement

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- Provide configurable priority levels
- Support P-channel connection
- Display interrupts with status

3.6.3. Block Diagram

The following figure displays the block diagram of PMU.

3.6.4. Function Description

Clock and Reset

PCLK and PRESETN are corresponding to registers. POR and **pad_reset** can reset the whole module.

Power Mode Switch

The PMU module accept software or hardware encourage to switch the power mode. only two operation to launch a power mode switching: Configure power mode, and turn-on or turn-off sequence configuration. PMU module launch p-channel (maskable) and PMU cell sequence.

Programming model:

SW encourage Turn-on sequence

1. Configure the register SW turn-on power mode (offset 0x0c), write the bit 1 which power domain will be turn-on, write the others 0;
2. Write the SW Turn-on command sequence. Write the register Software encourage (offset 0x44) 0xff –> 0x05 –> 0x50

SW encourage Turn-off sequence

1. Configure the register SW turn-off power mode (offset 0x10), write the bit 1 which power domain will be turn-off, write the others 0;
2. Write the SW Turn-off command sequence. write the register Software encourage (offset 0x44) 0xff –> 0x0a –> 0xa0

HW encourage Turn-on sequence

1. Configure the register HW turn-on power mode (offset 0x5c), write the bit 1 which power domain will be turn-on, write the others 0;
2. Configure the mask of HW event. write the Hardware Event Turn-on Mask (0x04) bit to 0 to enable HW event trigger off a Turn-on sequence. See Hardware Event Turn-On Mask *(on page 499)* for more information.

Interrupt

PMU has a interrupt type with 9 event status. See the register Interrupts Status (offset 0x8c) for more information.

3.6.5. Register Description

The PMU of JH-7110 has the following registers.

Hardware Event Turn-On Mask

The following table displays information on the hardware event turn-on mask Control Registers.

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Table 3-12 Hardware Event Turn-On Mask Register Description

Offset Address: 0x4				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	Hard_event_0_on_mask	RW	0	RTC event encourage turn-on sequence • 1: mask hardware event • 0: enable hardware event
[1]	Hard_event_1_on_mask	RW	0	GMAC event encourage turn-on sequence • 1: mask hardware event • 0: enable hardware event
[2]	Hard_event_2_on_mask	RW	0	RFU • 1: mask hardware event • 0: enable hardware event
[3]	Hard_event_3_on_mask	RW	0	RGPIO0 event encourage turn-on sequence • 1: mask hardware event • 0: enable hardware event
[4]	Hard_event_4_on_mask	RW	0	RGPIO1 event encourage turn-on sequence • 1: mask hardware event • 0: enable hardware event
[5]	Hard_event_5_on_mask	RW	0	RGPIO2 event encourage turn-on sequence • 1: mask hardware event • 0: enable hardware event
[6]	Hard_event_6_on_mask	RW	0	RGPIO3 event encourage turn-on sequence • 1: mask hardware event • 0: enable hardware event
[7]	Hard_event_7_on_mask	RW	0	GPU event • 1: mask hardware event • 0: enable hardware event
[8:31]	Reserved			Reserved

Software Turn-On Power Mode

The software turn-on power mode Control Registers are used to configure the power-on mode of the destination via software.

The following table displays information on the software turn-on power mode Control Registers.

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Table 3-13 Software Turn-On Power Mode Register Description

Offset Address: 0xc				
Default: 0x003				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	systop_power_mode	RW	0x1	SYSTOP turn-on power mode
[1]	cpu_power_mode	RW	0x1	CPU turn-on power mode
[2]	gpua_power_mode	RW	0x0	GPUA turn-on power mode
[3]	vdec_power_mode	RW	0x0	VDEC turn-on power mode
[4]	vout_power_mode	RW	0x0	VOUT turn-on power mode
[5]	isp_power_mode	RW	0x0	ISP turn-on power mode
[6]	venc_power_mode	RW	0x0	VENC turn-on power mode
[31:7]	Reserved			Reserved

Software Turn-Off Power Mode

The software turn-on power mode Control Registers are used to configure the power-off mode of the destination via software.

The following table displays information on the software turn-off power mode Control Registers.

Table 3-14 Software Turn-Off Power Mode Register Description

Offset Address: 0x10				
Default: 0x00				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	systop_power_mode	RW	0x0	SYSTOP turn-on power mode
[1]	cpu_power_mode	RW	0x0	CPU turn-on power mode
[2]	gpua_power_mode	RW	0x0	GPUA turn-on power mode
[3]	vdec_power_mode	RW	0x0	VDEC turn-on power mode
[4]	vout_power_mode	RW	0x0	VOUT turn-on power mode
[5]	isp_power_mode	RW	0x0	ISP turn-on power mode
[6]	venc_power_mode	RW	0x0	VENC turn-on power mode
[31:7]	Reserved			Reserved

Threshold Sequence Timeout

The following table displays information on the threshold sequence timeout Control Registers.

Table 3-15 Threshold Sequence Timeout Register Description

Offset Address: 0x14				
Default: 0xffff				
Bit	**Name**	**Access**	**Default**	**Description**
[15:0]	timeout_seq_thd	RW	0xffff	Threshold sequence timeout
[31:16]	Reserved			Reserved

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Powerdomain Cascade 0

The following table displays information on the Powerdomain Cascade 0 Control Registers.

Table 3-16 Powerdomain Cascade 0 Register Description

Offset Address: 0x18				
Default: 0x04008402				
Bit	**Name**	**Access**	**Default**	**Description**
[4:0]	pd0_off_cas	RW	0x2	Power domain 0 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[9:5]	pd0_on_cas	RW	0x0	Power domain 0 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[14:10]	pd1_off_cas	RW	0x1	Power domain 1 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[19:15]	pd1_on_cas	RW	0x1	Power domain 1 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[24:20]	pd2_off_cas	RW	0x0	Power domain 2 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[29:25]	pd2_on_cas	RW	0x2	Power domain 2 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[30:31]	Reserved			Reserved

Powerdomain Cascade 1

The following table displays information on the Powerdomain Cascade 1 Control Registers.

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Table 3-17 Powerdomain Cascade 1 Register Description

Offset Address: 0x1c				
Default: 0x04010040				
Bit	**Name**	**Access**	**Default**	**Description**
[4:0]	pd3_off_cas	RW	0x0	Power domain 3 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[9:5]	pd3_on_cas	RW	0x2	Power domain 3 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[14:10]	pd4_off_cas	RW	0x0	Power domain 4 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[19:15]	pd4_on_cas	RW	0x2	Power domain 4 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[24:20]	pd5_off_cas	RW	0x0	Power domain 5 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[29:25]	pd5_on_cas	RW	0x2	Power domain 5 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[30:31]	Reserved			Reserved

Powerdomain Cascade 2

The following table displays information on the Powerdomain Cascade 2 Control Registers.

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Table 3-18 Powerdomain Cascade 2 Register Description

Offset Address: 0x20				
Default: 0x04010040				
Bit	**Name**	**Access**	**Default**	**Description**
[4:0]	pd6_off_cas	RW	0x0	Power domain 6 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[9:5]	pd6_on_cas	RW	0x2	Power domain 6 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[14:10]	pd7_off_cas	RW	0x0	Power domain 7 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[19:15]	pd7_on_cas	RW	0x2	Power domain 7 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[24:20]	pd8_off_cas	RW	0x0	Power domain 8 turn-off cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[29:25]	pd8_on_cas	RW	0x2	Power domain 8 turn-on cascade. The register value indicates the power-off sequence of this domain. 0 means the highest priority. System only accepts value from 0 to 7, any other value is invalid.
[30:31]	Reserved			Reserved

Software Encourage

The following table displays information on the Software Encourage Control Registers.

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Table 3-19 Software Encourage Register Description

Offset Address: 0x44				
Default: 0x00				
Bit	**Name**	**Access**	**Default**	**Description**
[7:0]	sw_encourage	RW	0x00	Software encouragement
[8:31]	Reserved			Reserved

TIMER Interrupt Mask Register

The following table displays information on the TIMER Interrupt Mask Register Control Registers.

Table 3-20 TIMER Interrupt Mask Register Description

Offset Address: 0x48				
Default: 0x1ff				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	seq_done_mask	RW	0x1	Mask the sequence complete event. • 0: mask • 1: Unmask
[1]	hw_req_mask	RW	0x1	Mask the hardware encouragement request. • 0: mask • 1: Unmask
[2:3]	sw_fail_mask	RW	0x1	Mask the software encouragement failure event. • 0: mask • 1: Unmask
[4:5]	hw_fail_mask	RW	0x1	Mask the hardware encouragement failure event. • 0: mask • 1: Unmask
[8:6]	pch_fail_mask	RW	0x1	Mask the P-channel failure event. • 0: mask • 1: Unmask
[31:9]	Reserved			Reserved

P-channel Bypass

The following table displays information on the P-channel Bypass Control Registers.

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Table 3-21 P-channel Bypass Register Description

Offset Address: 0x4c				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	pch_bypass	RW	0x0	Bypass p-channel. • 0: Enable p-channel • 1: Bypass p-channel
[1:31]	Reserved			Reserved

P-channel PSTATE

The following table displays information on the P-channel Bypass Control Registers.

Table 3-22 P-channel Bypass Register Description

Offset Address: 0x50				
Default: 0Xffff_ffff				
Bit	**Name**	**Access**	**Default**	**Description**
[4:0]	pch_pstate	RW	0x1f	P-channel state set
[31:5]	Reserved			Reserved

P-channel Timeout Threshold

The following table displays information on the P-channel timeout threshold Control Registers.

Table 3-23 P-channel Timeout Threshold Register Description

Offset Address: 0x54				
Default: 0x01				
Bit	**Name**	**Access**	**Default**	**Description**
[7:0]	lp_timeout	RW	0x01	P-channel waiting device acknowledge time-out.
[8:31]	Reserved			Reserved

LP Cell Control Timeout Threshold

The following table displays information on the LP Cell Control timeout threshold Control Registers.

Table 3-24 LP Cell Control Timeout Threshold Register Description

Offset Address: 0x58				
Default: 0x01				
Bit	**Name**	**Access**	**Default**	**Description**
[7:0]	lp_timeout	RW	0x01	LP Cell Control signal waiting carriers ac-knowledge timeout.
[8:31]	Reserved			Reserved

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Hardware Turn-On Power Mode

The hardware turn-on power mode Control Registers are used to configure the power-on mode of the destination via hardware.

The following table displays information on the hardware turn-on power mode Control Registers.

Table 3-25 Hardware Turn-On Power Mode Register Description

Offset Address: 0x5c				
Default: 0x003				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	systop_power_mode	RW	0x1	SYSTOP turn-on power mode
[1]	cpu_power_mode	RW	0x1	CPU turn-on power mode
[2]	gpua_power_mode	RW	0x0	GPUA turn-on power mode
[3]	vdec_power_mode	RW	0x0	VDEC turn-on power mode
[4]	vout_power_mode	RW	0x0	VOUT turn-on power mode
[5]	isp_power_mode	RW	0x0	ISP turn-on power mode
[6]	venc_power_mode	RW	0x0	VENC turn-on power mode
[31:7]	Reserved			Reserved

Current Power Mode

The following table displays information on the current power mode Control Registers.

Table 3-26 Current Power Mode Register Description

Offset Address: 0x80				
Default: 0x103				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	systop_power_mode	RW	0x1	SYSTOP turn-on power mode
[1]	cpu_power_mode	RW	0x1	CPU turn-on power mode
[2]	gpua_power_mode	RW	0x0	GPUA turn-on power mode
[3]	vdec_power_mode	RW	0x0	VDEC turn-on power mode
[4]	vout_power_mode	RW	0x0	VOUT turn-on power mode
[5]	isp_power_mode	RW	0x0	ISP turn-on power mode
[6]	venc_power_mode	RW	0x0	VENC turn-on power mode
[31:7]	Reserved			Reserved

Current Sequence State

The following table displays information on the current sequence state Control Registers.

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Table 3-27 Current Sequence State Register Description

Offset Address: 0x84				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[1:0]	powermode_cur	RO	0x0	Current sequence state.
[2:31]	Reserved			Reserved

Event Status

The following table displays information on the event status Control Registers.

Table 3-28 PMU Event Status Register Description

Offset Address: 0x88				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	seq_done_event	RO	0x1	Sequence complete.
[1]	hw_req_event	RO	0x1	Hardware encouragement request.
[2:3]	sw_fail_event	RO	0x1	Software encouragement failure.
[4:5]	hw_fail_event	RO	0x1	Hardware encouragement failure.
[8:6]	pch_fail_event	RO	0x1	P-channel failure.
[31:9]	Reserved			Reserved

Interrupt Status

The following table displays information on the interrupt status Control Registers.

Table 3-29 PMU Event Status Register Description

Offset Address: 0x8c				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	seq_done_event	RO	0x1	Sequence complete.
[1]	hw_req_event	RO	0x1	Hardware encouragement request.
[2:3]	sw_fail_event	RO	0x1	Software encouragement failure.
[4:5]	hw_fail_event	RO	0x1	Hardware encouragement failure.
[8:6]	pch_fail_event	RO	0x1	P-channel failure.
[31:9]	Reserved			Reserved

Hardware Event Record

The following table displays information on the hardware event record Control Registers.

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Table 3-30 Hardware Event Record Register Description

Offset Address: 0x90				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[7:0]	hw_event_crd	RO	0x0	Hardware event record.
[8:31]	Reserved			Reserved

Hardware Event Type Record

The following table displays information on the hardware event type record Control Registers.

Table 3-31 Hardware Event Type Record Register Description

Offset Address: 0x94				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	encourage_type_crd	RO	0x0	Hardware/Software encouragement type record. • 0: Software • 1: Hardware
[1:31]	Reserved			Reserved

P-channel PACTIVE status

The following table displays information on the P-channel PACTIVE Control Registers.

Table 3-32 P-channel PACTIVE Register Description

Offset Address: 0x98				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[10:0]	pch_active	RO	0x0	P-channel PACTIVE status
[31:11]	Reserved			Reserved

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4. Image Subsystem

4.1. ISP

Compared with the previous version, JH-7110 implements ISP 2.0 which brings about image quality improvement, geographic distortion correction, video stabilization, and overlay functions to extend the range of possible applications.

4.1.1. Overview

4.1.2. Feature

The ISP-RGB of JH-7110 has the following features.

- Sensor Interface
    - Support up to 1080P @30fps CMOS RGGB image sensor with the output format of RAW
    - Support 1 MIPI and 1 DVP sensor input interface
    - Support 12-bit sensor data input
- Image processing engine
    - Built-in color pattern generation
    - Sensor black level compensation
    - Defective pixel correction
    - R/G/B LUT for sensor linearisation correction
    - Image analysis for AE, AWB, and AF
    - Programmable histogram analysis
    - White balance control
    - Lens shading compensation
    - Color shading compensation
    - CMOS sensor spatial crosstalk cancellation (Gr and Gb balance filter)
    - Advanced Bayer CFA color interpolation
    - False-color suppression
    - Advanced edge control and enhancement
    - R/G/B Gamma LUT
    - Color correction matrix
    - Color space conversion
    - Brightness/contrast and hue/saturation adjustment
    - Global tone mapping
    - Spatial noise reduction
- Back-end processing
    - Seamless digital scale down from 1/4 × to 1 ×
    - Support up to 3 channel video streaming

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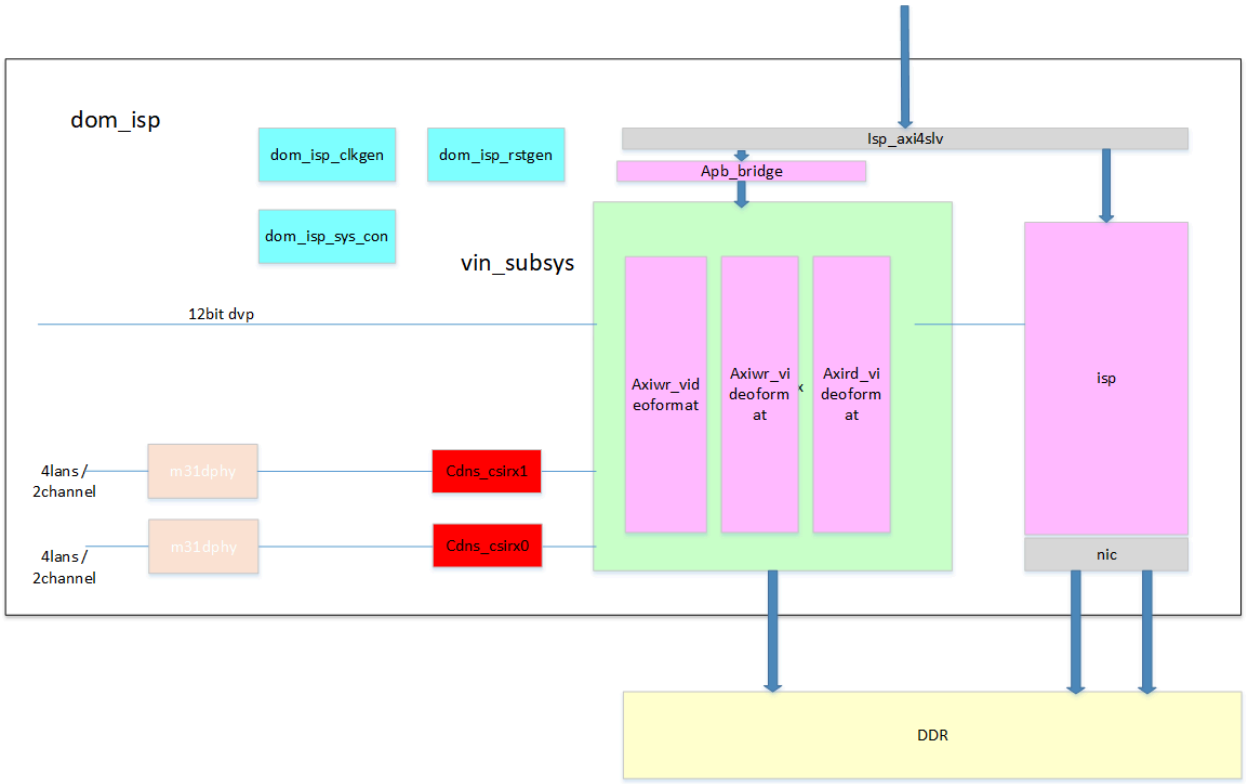
Note:
5M Px is only supported with the following data path "Sensor → VIN (max 4K) → DDR", the sensor data output is YUV420 or YUV 422.

4.1.3. Block Diagram

In the JH-7110 platform, ISP is called **dom_isp**.

The block diagram of the subsystem is displayed in the following diagram.

Figure 4-1 ISP Block Diagram



4.1.4. Clock and Reset Specification

Clock Specification

The clock specification of ISP are displayed in the following sheet.

Table 4-1 ISP Clock Specification

Module	Clock	Internal	Default Freq (MHz)	Max Freq (MHz)	Typ. Freq (MHz)
dom_isp_syscon	clk_isp_2x	TRUE	0	614.4	614.4
	clk_isp_axi	TRUE	0	307.2	307.2
	clk_dom4_apb_func	TRUE	0	51.2	51.2
dom_isp_crg	clk_mipi_rx0_pxl	TRUE	0	307.2	204.8
	clk_bist_apb	TRUE	50	50	50
	u3_pclk_mux.func_pclk	FALSE	0	51.2	51.2

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Table 4-1 ISP Clock Specification (continued)

Module	Clock	Internal	Default Freq (MHz)	Max Freq (MHz)	Typ. Freq (MHz)
	u3_pclk_mux.bist_pclk	FALSE	50	50	50
	clk_dom4_apb	TRUE	0	51.2	51.2
	clk_dvp_inv	TRUE	148.5	200	148.5
u0_vin	u0_m31dphy.cfgclk_in	FALSE	0	153.6	102.4
	u0_m31dphy.refclk_in	FALSE	0	102.4	51.2
	u0_m31dphy.txclkesc_lan0	FALSE	0	40.96	20.48
	u0_vin.pclk_free	FALSE	0	51.2	51.2
	u0_vin.pclk	FALSE	0	51.2	51.2
	u0_vin.sys_clk	FALSE	0	614.4	307.2
	u0_vin.pixel_clk_if0	FALSE	0	307.2	204.8
	u0_vin.pixel_clk_if1	FALSE	0	307.2	204.8
	u0_vin.pixel_clk_if2	FALSE	0	307.2	204.8
	u0_vin.pixel_clk_if3	FALSE	0	307.2	204.8
	u0_vin.clk_p_axird	FALSE	0	307.2	204.8
	u0_vin.clk_p_axiwr	FALSE	0	307.2	204.8
	u0_vin.ACLK	FALSE	0	307.2	307.2
	u0_ispv2_top_wrapper.clk_isp_axi_in	FALSE	0	307.2	307.2
	u0_ispv2_top_wrapper.clk_isp_x2	FALSE	0	614.4	614.4
u0_ispv2_top_wrapper	u0_ispv2_top_wrapper.clk_isp	FALSE	0	307.2	307.2
	u0_ispv2_top_wrapper.clk_p	FALSE	0	307.2	204.8
	u0_ispv2_top_wrapper.clk_c	FALSE	0	307.2	204.8
dom_isp_crg	u0_crg.pclk	TRUE	0	51.2	51.2
dom_isp_syscon	u0_syscon.pclk	FALSE	0	51.2	51.2
m31dphy_apbcfg	u0_m31dphy_apbcfg.pclk	FALSE	0	51.2	51.2
axi2apb_bridge	u0_axi2apb_bridge.clk_dom4_apb	FALSE	0	51.2	51.2
	u0_axi2apb_bridge.isp_axi4slv_clk	FALSE	0	307.2	307.2

Reset Specification

The reset specification of ISP are displayed in the following sheet.

Table 4-2 ISP Reset Specification

Module	Reset	Soft	rootReset0
u0_isp	u0_ispv2_top_wrapper.rst_p	TRUE	dom_isp_top.ip_top_reset_n
	u0_ispv2_top_wrapper.rst_c	TRUE	dom_isp_top.ip_top_reset_n

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Table 4-2 ISP Reset Specification (continued)

Module	Reset	Soft	rootReset0
	u0_ispv2_top_wrapper.rstn_isp	FALSE	dom_isp_top.rstn_isp_axi
	u0_ispv2_top_wrapper.rstn_isp_axi	FALSE	dom_isp_top.rstn_isp_axi
	u0_m31dphy.hw_rstn	TRUE	dom_isp_top.ip_top_reset_n
	u0_m31dphy.RSTB09_ALWAYS_ON	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.rst_n_pclk	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.rst_n_pixel_clk_if0	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.rst_n_pixel_clk_if1	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.rst_n_pixel_clk_if2	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.rst_n_pixel_clk_if3	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.rst_n_sys_clk	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.rst_p_axird	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.rst_p_axiwr	TRUE	dom_isp_top.ip_top_reset_n
	u0_vin.ARESETn	FALSE	dom_isp_top.rstn_isp_axi
	u0_axi2apb_bridge.ip_top_reset_n	FALSE	dom_isp_top.ip_top_reset_n
	u0_axi2apb_bridge.isp_axi4slv_rstn	FALSE	dom_isp_top.rstn_isp_axi
	u0_crg.func_resetn	FALSE	dom_isp_top.ip_top_reset_n
	u0_crg.presetn	FALSE	dom_isp_top.ip_top_reset_n
	u0_syscon.presetn	FALSE	dom_isp_top.ip_top_reset_n
	u0_m31dphy_apbcfg.presetn	FALSE	dom_isp_top.ip_top_reset_n

Detailed Information

If you still need more information on the clock and reset specifications of ISP, contact StarFive for the following documentation.

- *ISP subsystem clock and reset specification*

4.1.5. Control Registers

4.1.5.1. CRG

The CRG of ISP RGB has the following registers.

clk_dom4_apb_func

Table 4-3 clk_dom4_apb_func Register Description

Offset Address: 16'h0			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved

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Table 4-3 clk_dom4_apb_func Register Description (continued)

Offset Address: 16'h0			
Access: RW			
Bit	**Name**	**Default**	**Description**
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h6	Clock divider coefficient: • Max: 15 • Default: 6 • Min: 6 • Typical: 6

clk_mipi_rx0_pxl

Table 4-4 clk_mipi_rx0_pxl Register Description

Offset Address: 16'h4			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h3	Clock divider coefficient: • Max: 8 • Default: 3 • Min: 2 • Typical: 3

clk_dvp_inv

Table 4-5 clk_dvp_inv Register Description

Offset Address: 16'h8			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	clk_polarity	1	• 1: clock inverter • 0: clock buffer
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_m31dphy_cfgclk_in

Table 4-6 clk_u0_m31dphy_cfgclk_in Register Description

Offset Address: 16'hc			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h6	Clock divider coefficient: • Max: 16 • Default: 6 • Min: 4 • Typical: 6

clk_u0_m31dphy_refclk_in

Table 4-7 clk_u0_m31dphy_refclk_in Register Description

Offset Address: 16'h10			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h12	Clock divider coefficient: • Max: 16 • Default: 12 • Min: 6 • Typical: 12

clk_u0_m31dphy_txclkesc_lan0

Table 4-8 clk_u0_m31dphy_refclk_in Register Description

Offset Address: 16'h14			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h30	Clock divider coefficient:

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Table 4-8 clk_u0_m31dphy_refclk_in Register Description (continued)

Offset Address: 16'h14			
Access: RW			
Bit	**Name**	**Default**	**Description**
			• Max: 60 • Default: 30 • Min: 15 • Typical: 30

clk_u0_vin_pclk

Table 4-9 clk_u0_vin_pclk Register Description

Offset Address: 16'h18			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_vin_sys_clk

Table 4-10 clk_u0_vin_sys_clk Register Description

Offset Address: 16'h1c			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h2	Clock divider coefficient: • Max: 8 • Default: 2 • Min: 1 • Typical: 2

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clk_u0_vin_pixel_clk_if0

Table 4-11 clk_u0_vin_pixel_clk_if0 Register Description

Offset Address: 16'h20			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_vin_pixel_clk_if1

Table 4-12 clk_u0_vin_pixel_clk_if1 Register Description

Offset Address: 16'h24			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_vin_pixel_clk_if2

Table 4-13 clk_u0_vin_pixel_clk_if2 Register Description

Offset Address: 16'h28			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_vin_pixel_clk_if3

Table 4-14 clk_u0_vin_pixel_clk_if3 Register Description

Offset Address: 16'h2c			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_vin_clk_p_axiwr

Table 4-15 clk_u0_vin_clk_p_axiwr Register Description

Offset Address: 16'h30			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6"h0	Clock multiplexing selector: • clk_mipi_rx0_pxl • clk_dvp_inv
[0:23]	Reserved	0	Reserved

clk_u0_ispv2_top_wrapper_clk_c

Table 4-16 clk_u0_ispv2_top_wrapper_clk_c Register Description

Offset Address: 16'h34			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	1	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6"h0	Clock multiplexing selector: • clk_mipi_rx0_pxl • clk_dvp_inv
[0:23]	Reserved	0	Reserved

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Software_RESET_assert0_addr_assert_sel

Table 4-17 Software_RESET_assert0_addr_assert_sel Register Description

Offset Address: 16'h38			
Access: RW			
Bit	**Name**	**Default**	**Description**
[0]	rst_u0_ispv2_top_wrapper_rst_p	1	• 1: Assert reset • 0: De-assert reset
[1]	rst_u0_ispv2_top_wrapper_rst_c	1	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_m31dphy_hw_rstn	1	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_m31dphy_RSTB09_ALWAYS_ON	1	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_vin_rst_n_pclk	1	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_vin_rst_n_pixel_clk_if0	1	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_vin_rst_n_pixel_clk_if1	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u0_vin_rst_n_pixel_clk_if2	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u0_vin_rst_n_pixel_clk_if3	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_vin_rst_n_sys_clk	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_vin_rst_p_axird	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_vin_rst_p_axiwr	1	• 1: Assert reset • 0: De-assert reset
[31:12]	Reserved	0	Reserved

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ISPCRG_RESET_STATUS

Table 4-18 ISPCRG_RESET_STATUS Register Description

Offset Address: 16'h3c			
Access: RW			
Bit	**Name**	**Default**	**Description**
[0]	rst_u0_ispv2_top_wrapper_rst_p	1	• 1: Assert reset • 0: De-assert reset
[1]	rst_u0_ispv2_top_wrapper_rst_c	1	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_m31dphy_hw_rstn	1	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_m31dphy_RSTB09_ALWAYS_ON	1	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_vin_rst_n_pclk	1	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_vin_rst_n_pixel_clk_if0	1	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_vin_rst_n_pixel_clk_if1	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u0_vin_rst_n_pixel_clk_if2	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u0_vin_rst_n_pixel_clk_if3	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_vin_rst_n_sys_clk	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_vin_rst_p_axird	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_vin_rst_p_axiwr	1	• 1: Assert reset • 0: De-assert reset
[31:12]	Reserved	0	Reserved

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4.1.5.2. SYSCON

The SYSCON of ISP RGB has the following registers.

SYSCONSAIF__SYSCFG_0

Table 4-19 SYSCONSAIF__SYSCFG_0 Register Description

Offset Address: 0x0				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[1:0]	u0_vin_SCFG_sram_config	RW	0x0	Reserved
[2]	u0_vin_cnfg_axi_dvp_en	RW	0x0	• 0: Output to AXI is DVP. • 1: Output to AXI is MIPI.
[13:3]	u0_vin_cnfg_axird_axi_cnt_-end	RW	0x0	The valid pixel of the AXI image. (1 pixel equals to 64 bit.)
[31:14]	Reserved	None	0x0	Reserved

SYSCONSAIF__SYSCFG_4

Table 4-20 SYSCONSAIF__SYSCFG_4 Register Description

Offset Address: 0x4				
Access: RW				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_vin_cnfg_axird_end_addr	RW	0x0	The start address of the next frame.

SYSCONSAIF__SYSCFG_8

Table 4-21 SYSCONSAIF__SYSCFG_8 Register Description

Offset Address: 0x8				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	u0_vin_cnfg_axird_intr_clean	RW	0x0	Use this bit to clean the AXI output interrupt. Write 1 then write 0 to execute the cleaning.
[1]	u0_vin_cnfg_axird_intr_mask	RW	0x0	Use this bit to mask the AXI output interrupt.
[13:2]	u0_vin_cnfg_axird_line_cnt_-end	RW	0x0	This bit represents the valid end pixel of the AXI input test image line.
[25:14]	u0_vin_cnfg_axird_line_cnt_-start	RW	0x0	This bit represents the valid start pixel of the AXI input test image line.
[31:26]	Reserved	None	0x0	Reserved

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SYSCONSAIF__SYSCFG_12

Table 4-22 SYSCONSAIF__SYSCFG_12 Register Description

Offset Address: 0xc				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[12:0]	u0_vin_cnfg_axird_pix_cnt_-end	RW	0x0	This bit represents the valid end pixel of the AXI input test image line.
[25:13]	u0_vin_cnfg_axird_pix_cnt_s-tart	RW	0x0	This bit represents the valid start pixel of the AXI input test image line.
[27:26]	u0_vin_cnfg_axird_pix_ct	RW	0x0	• 00: 1 64-bit equals to 2 pixels • 01: 1 64-bit equals to 4 pixels • 10: 1 64-bit equals to 8 pixels
[31:28]	Reserved	None	0x0	Reserved

SYSCONSAIF__SYSCFG_16

Table 4-23 SYSCONSAIF__SYSCFG_16 Register Description

Offset Address: 0x10				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_vin_cnfg_axird_start_addr	RW	0x0	This bit represents the valid start address of the AXI input test image's first line.

SYSCONSAIF__SYSCFG_20

Table 4-24 SYSCONSAIF__SYSCFG_20 Register Description

Offset Address: 0x14				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:3]	u0_vin_cnfg_axiwr0_chan-nel_sel	RW	0x0	Select 1 channel output of the 8 MIPI chan-nels
[4]	u0_vin_cnfg_axiwr0_en	RW	0x0	Set this bit to 1 to enable the image output to AXI.
[31:5]	Reserved	None	0x0	Reserved

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SYSCONSAIF__SYSCFG_24

Table 4-25 SYSCONSAIF__SYSCFG_24 Register Description

Offset Address: 0x18				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_vin_cnfg_axiwr0_end_addr	RW	0x0	This bit represents the start address of the next frame.

SYSCONSAIF__SYSCFG_28

Table 4-26 SYSCONSAIF__SYSCFG_28 Register Description

Offset Address: 0x1c				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	u0_vin_cnfg_axiwr0_intr_clean	RW	0x0	Use this bit to clean the AXI output interrupt. Write 1 then write 0 to execute the cleaning.
[1]	u0_vin_cnfg_axiwr0_intr_mask	RW	0x0	Use this bit to mask the AXI output interrupt.
[12:2]	u0_vin_cnfg_axiwr0_pix_cnt_end	RW	0x0	This bit represents the valid end pixel of the AXI input test image line.
[14:13]	u0_vin_cnfg_axiwr0_pix_ct	RW	0x0	• 00: 1 64-bit equals to 2 pixels • 01: 1 64-bit equals to 4 pixels • 10: 1 64-bit equals to 8 pixels
[16:15]	u0_vin_cnfg_axiwr0_pixel_high_bit_sel	RW	0x0	When you configure the above bit as "10" - 1 64-bit equals to 8 pixels, the 8 pixels will use some of the RAW data: • 00: pix_data[7:0] • 01: pix_data[9:2] • 10: pix_data[11:4] • 11: pix_data[13:6]
[31:17]	Reserved	None	0x0	Reserved

SYSCONSAIF__SYSCFG_32

Table 4-27 SYSCONSAIF__SYSCFG_32 Register Description

Offset Address: 0x20				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_vin_cnfg_axiwr0_start_addr	RW	0x0	This bit represents the start address of the AXI output image.

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SYSCONSAIF__SYSCFG_36

Table 4-28 SYSCONSAIF__SYSCFG_36 Register Description

Offset Address: 0x24				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	u0_vin_cnfg_color_bar_en	RW	0x0	Set this bit to 1 to use the color bar for test.
[1]	u0_vin_cnfg_dvp_hs_pos	RW	0x0	Use DVP to AXI • 1: HS is high valid. • 0: HS is low valid.
[2]	u0_vin_cnfg_dvp_swap_en	RW	0x0	Set this bit to 1 to enable DVP swap.
[3]	u0_vin_cnfg_dvp_vs_pos	RW	0x0	Use DVP to AXI • 1: VS is high valid. • 0: VS is low valid.
[4]	u0_vin_cnfg_gen_en_axird	RW	0x0	Set this bit to use AXI input for ISP and generate the test image.
[5]	u0_vin_cnfg_isp_dvp_en0	RW	0x0	Set this bit to use DVP input for ISP.
[6:7]	u0_vin_cnfg_mipi_byte_en_isp0	RW	0x0	Set this bit to 1 for dvp_clk_inv, the DVP clock inverter register.
[11:8]	u0_vin_cnfg_mipi_channel_sel0	RW	0x0	Select 1 channel output of the 8 MIPI channels
[12]	u0_vin_cnfg_p_i_mipi_header_en0	RW	0x0	Set this bit to 1 to add 10 bits to bit 2, so 1 pixel equals to 12 bits.
[16:13]	u0_vin_cnfg_pix_num	RW	0x0	VIN AXI to ISP MIPI port, 12-bit data configuration: • 2b'00: axi_data[11:0] • 2b'01: {axi_data[9:0], 2b'0} • 2b'10: {axi_data[7:0], 4b'0} • 2b'11: {axi_data[5:0], 6b'0}
[26:17]	u0_vin_generic_sp	RO	0x0	This configuration is not used by JH-7110.
[31:27]	Reserved	None	0x0	Reserved

SYSCONSAIF__SYSCFG_40

Table 4-29 SYSCONSAIF__SYSCFG_40 Register Description

Offset Address: 0x28				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[15:0]	u0_vin_test_generic_ctrl	RO	0x0	This configuration is not used by JH-7110.
[31:16]	u0_vin_test_generic_status	RW	0x0	This configuration is not used by JH-7110.

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4.1.6. More Information

ISPV2

If you still need more information on the ISPV2 of JH-7110, contact StarFive and request the following documentation.

- ISP V2 reference: *ISP V2.0 Development Plan*
- VIN_syscon_register reference: vin_syscon_register.csv
- M31dphy_register reference: m31dphy_apbcfg.csv

cdns_csi2Rx

If you still need more information on the cdns_csi2Rx of JH-7110, contact StarFive and request the following documentation.

- *MIPI-CSI2 v1.3 RX Controller (CSI2RX) User Guide*

MIPI RX DPHY

If you still need more information on the MIPI RX DPHY of JH-7110, contact StarFive and request the following documentation.

- *M31DPHYRX611TL028D MIPI D-PHY Receiver of TSMC 28nm Logic 0.9V/1.8V High Performance Compact Plus Process*

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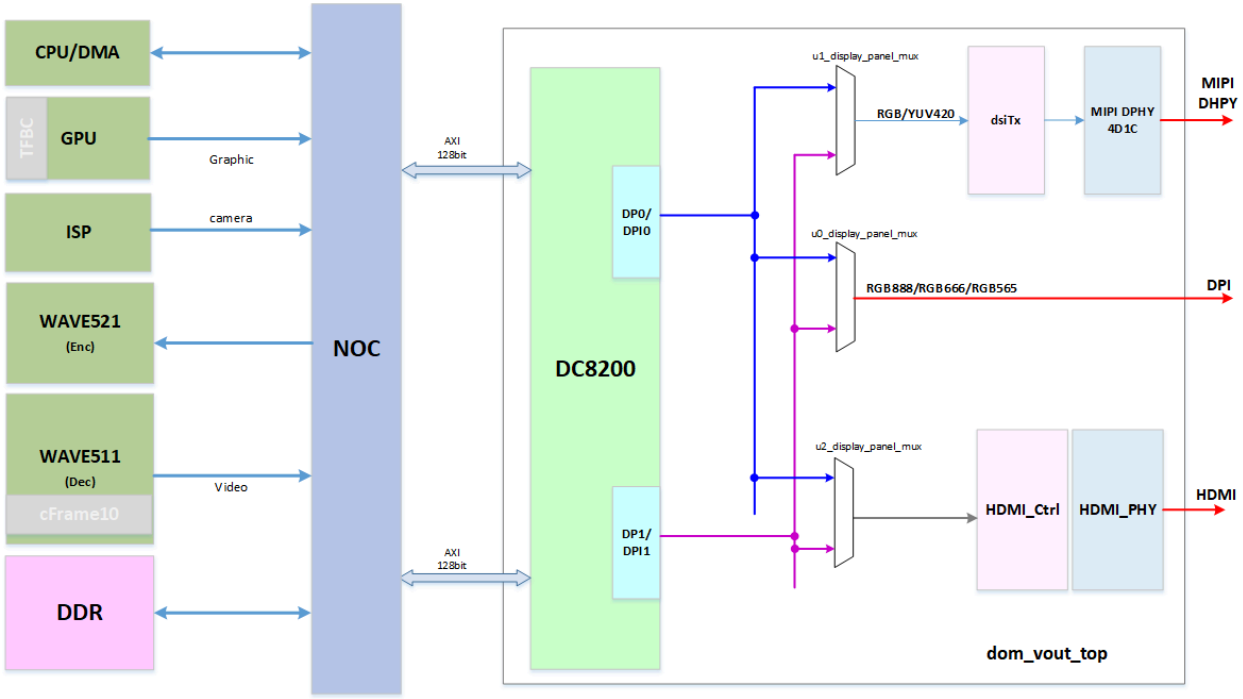
5. Display Subsystem

The display subsystem, named as dom_vout_top in the JH-7110 system, includes front-end video data capture, display controller and display interface, such as RGB IF, HDMI and MIPI.

5.1. Block Diagram

The block diagram of the display subsystem is displayed in following diagram.

Figure 5-1 Display Subsystem Block Diagram



Data Mapping

The DSI transmitter's pixel data could be from panel 0 or panel 1 interface of DC8200, and could be selected from DP or DPI interface. The RGB PAD and HDMI have similar mechanism.

Table 5-1 Display Subsystem Data Mapping

Destination	Supported Data Mapping	Comment
DPI to PAD	• DP0/DP1 or DPI0/1 is used, default DPI is used. • RGB24, RGB666 (CFG1), RGB565 (CFG1) when DPI is used.	For flexibility
DSI Tx Data from DC8200	• Both DPI and DP are supported. • YUV420 8-bit only (CFG3). • YUV422 8-bit only (CFG1).	Default DPI

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Table 5-1 Display Subsystem Data Mapping (continued)

Destination	Supported Data Mapping	Comment
HDMI Data from DC8200	• Both DP0 and DP1 are used for RGB and YUV. • YUV444 and YUV422 8-bit/10-bit (CFG1). • YUV420 8-bit/10-bit (CFG3).	DP by default, and DPI for back-up

5.2. Memory Map

The memory map of the display subsystem is displayed as the table below.

Table 5-2 Display Subsystem Memory Map

Base Address: 0x2940_0000				
AHB NO.	**Class**	**Module**	**Start Address**	**Size (KB)**
0	AHB	DC8200 AHB 0	0x00_0000	512
1	AHB	DC8200 AHB 1	0x08_0000	512
2	ahb2apb_sync	Reserved	0x10_0000	64
		Reserved	0x11_0000	64
		Reserved	0x12_0000	64
		Reserved	0x13_0000	64
		Reserved	0x14_0000	64
		Reserved	0x15_0000	64
		Reserved	0x16_0000	64
		Reserved	0x17_0000	64
		Reserved	0x18_0000	64
		u0_hdmitx	0x19_0000	64
		Reserved	0x1A_0000	64
		SYSCON	0x1B_0000	64
		CRG	0x1C_0000	64
		dsiTx(ahb2apb_sync)	0x1D_0000	64

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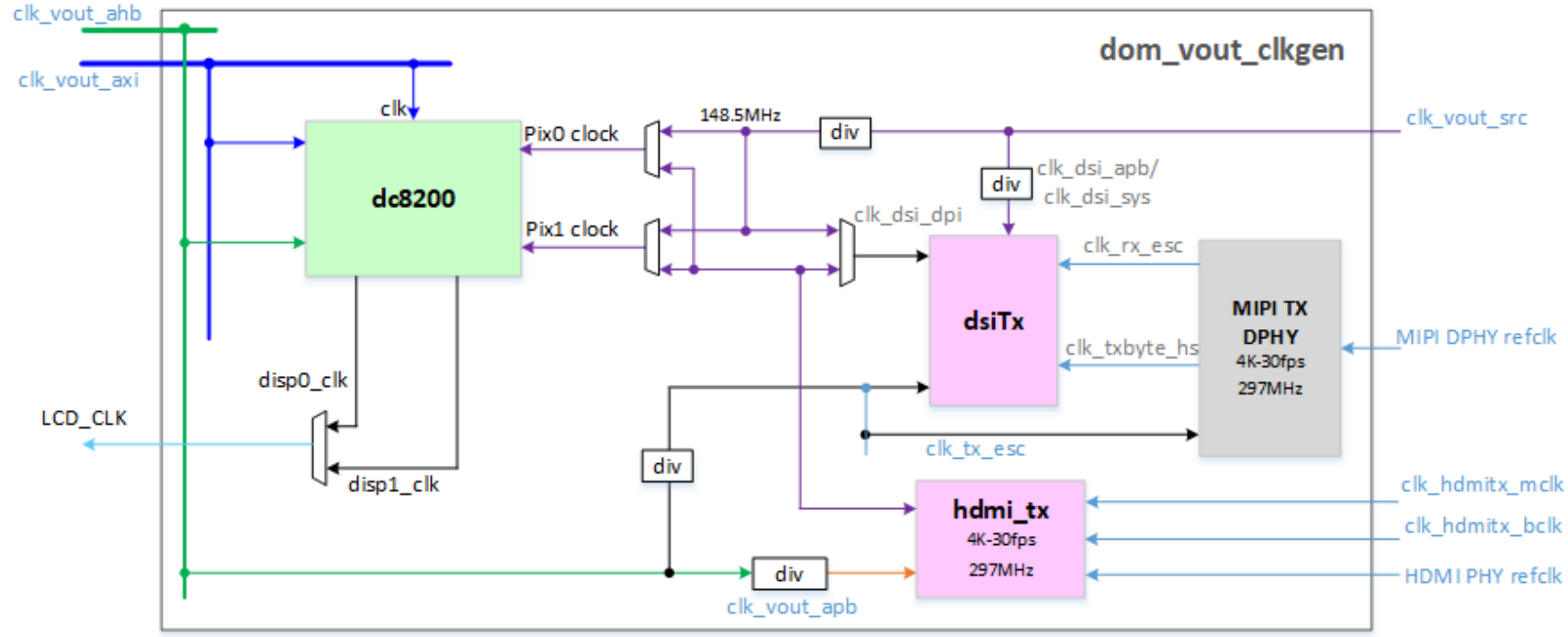
5.3. Clock and Reset

Block Diagram

The display subsystem has these clock source, source clock for whole display subsystem, MIPI TX DPHY"s PLL reference clock, HDMI PHY"s reference clock, four channel I2S transmitter bit clock.

The clock division architecture is shown in the following diagram.

Figure 5-2 Display Subsystem Clock and Reset Block Diagram



Specification

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The clock and reset specification of the display subsystem is displayed in the following table.

Table 5-3 Display Subsystem Clock and Reset Specification

Module	Clock	Internal	Default Freq (MHz)	Max Freq (MHz)	Typ. Freq (MHz)	Source0	Source1
	clk_disp_root	TRUE	0	1228.8	1228.8	dom_vout_top.clk_vout_src	
Source	clk_disp_axi	TRUE	0	614.4	614.4	dom_vout_top.clk_vout_axi	
	clk_disp_ahb	TRUE	0	204.8	204.8	dom_vout_top.clk_vout_ahb	
	clk_hdmi_phy_ref	TRUE	24	24	24	dom_vout_top.clk_hdmiphy_ref	
	clk_hdmitx0_mclk	TRUE	0	51.2	51.2	dom_vout_top.clk_hdmitx0_mclk	
	clk_hdmitx0_sck	TRUE	0	12.8	12.8	dom_vout_top.clk_hdmitx0_bclk	
	clk_hdmitx0_pixelclk	TRUE	0	297	0	u0_hdmi_tx.clk_pix	
	clk_mipi_dphy_ref	TRUE	12	12	12	dom_vout_top.clk_mipiphy_ref	
	clk_mipitx_dphy_rxesc	TRUE	0	10	0	u0_mipitx_dphy.clk_rxesc	
	clk_mipitx_dphy_txbytehs	TRUE	0	297	0	u0_mipitx_dphy.clk_txbytehs	
Divider	u0_pclk_mux.bist_pclk	FALSE	50	50	50	dom_vout_top.bist_pclk	
	clk_disp_apb	TRUE	0	51.2	51.2	u0_pclk_mux.pclk	
	clk_apb	TRUE	0	51.2	51.2	clk_disp_ahb	
	u0_pclk_mux.func_pclk	FALSE	0	51.2	51.2	clk_apb	
	clk_dc8200_pix0	TRUE	0	307.2	307.2	clk_disp_root	
	clk_dsi_sys	TRUE	0	307.2	307.2	clk_disp_root	
	clk_tx_esc	TRUE	0	20.48	17.07	clk_disp_ahb	
Bus	u0_dom_vout_crg.pclk	TRUE	0	51.2	51.2	clk_disp_apb	
	u0_dom_vout_syscon.pclk	FALSE	0	51.2	51.2	clk_disp_apb	
	u0_saif_amba_dom_vout_ah-b_dec.clk_ahb	FALSE	0	204.8	204.8	clk_disp_ahb	
	u0_ahb2apb.clk_ahb	FALSE	0	204.8	204.8	clk_disp_ahb	
	u0_p2p_async.clk_apbs	FALSE	0	51.2	51.2	clk_disp_apb	

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Table 5-3 Display Subsystem Clock and Reset Specification (continued)

Module	Clock	Internal	Default Freq (MHz)	Max Freq (MHz)	Typ. Freq (MHz)	Source0	Source1
	u0_p2p_async.clk_apbm	FALSE	0	307.2	307.2	clk_dsi_sys	
DC8200	u0_dc8200.clk_axi	FALSE	0	614.4	614.4	clk_disp_axi	
	u0_dc8200.clk_core	FALSE	0	614.4	614.4	clk_disp_axi	
	u0_dc8200.clk_ahb	FALSE	0	204.8	204.8	clk_disp_ahb	
	u0_dc8200.clk_pix0	FALSE	0	307.2	307.2	clk_dc8200_pix0	clk_hdmitx0_pixelclk
	u0_dc8200.clk_pix1	FALSE	0	307.2	307.2	clk_dc8200_pix0	clk_hdmitx0_pixelclk
	dom_vout_top.lcd_clk(gpio)	FALSE	0	74.25	0	u0_dc8200.clk_pix0_out	u0_dc8200.clk_pix1_-out
dsiTx	u0_cdns_dsiTx.clk_apb	FALSE	0	307.2	307.2	clk_dsi_sys	
	u0_cdns_dsiTx.clk_sys	FALSE	0	307.2	307.2	clk_dsi_sys	
	u0_cdns_dsiTx.clk_dpi	FALSE	0	307.2	307.2	clk_dc8200_pix0	clk_hdmitx0_pixelclk
	u0_cdns_dsiTx.clk_txesc	FALSE	0	20.48	17.07	clk_tx_esc	
	u0_cdns_dsiTx.clk_rxesc	FALSE	0	10	0	clk_mipitx_dphy_rxesc	
	u0_cdns_dsiTx.clk_txbytehs	FALSE	0	297	0	clk_mipitx_dphy_txbytehs	
mipitx DPHY	u0_mipitx_dphy.clk_txesc	FALSE	0	20.48	17.07	clk_tx_esc	
	u0_mipitx_dphy.clk_sys	FALSE	0	51.2	51.2	clk_disp_apb	
	u0_mipitx_dphy.clk_dphy_ref	FALSE	12	12	12	clk_mipi_dphy_ref	
	u0_mipitx_apbif.pclk	FALSE	0	51.2	51.2	clk_disp_apb	
HDMI	u0_hdmi_tx.clk_mclk	FALSE	0	51.2	51.2	clk_hdmitx0_mclk	
	u0_hdmi_tx.clk_bclk	FALSE	0	12.8	12.8	clk_hdmitx0_sck	
	u0_hdmi_tx.clk_sys	FALSE	0	51.2	51.2	clk_disp_apb	
	u0_hdmi_tx.clk_ref	FALSE	24	24	24	clk_hdmi_phy_ref	

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For more information on the specification, see vout_clkrst_spec.xlsx.

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5.4. Interrupt

The interrupt in the display subsystem is connected to both U74 and E24 core directly. All the interrupts of the module are connected to the display subsystem top, and then connected to CPU.

The interrupt bit map is shown in the following table.

Table 5-4 Display Subsystem Interrupts

Name	Order	Connection
vout_sys_int	0	DC8200 DC INT
	1	DC8200 SEC INT
	2	DC8200 MMU INT
	3	DSI
	4	u0_hdmi

5.5. Pixel Data Mapping

5.5.1. DC8200 Data Mapping

DC8200 has DP and DPI interfaces for each panel. The RGB data mapping in DP and DPI data is displayed in the following table. Only CFG1 supports RGB565 and RGB666 format.

Figure 5-3 DC8200 RGB Data Mapping

DPI Display Bit Mapping Options for display0Color

	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
30 bit R10G10B10	R7	R6	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DPI 24 bit							R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
DPI 18 bit Config 1													R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
DPI 18 bit Config 2									R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0
DPI 16 bit Config 1															R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
DPI 16 bit Config 2										R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0				B4	B3	B2	B1	B0
DPI 16 bit Config 3									R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0	

RGB Format Setting on the DP0/1_Data Signal

Configuration	Bits 2:0	47	...	43	42	41	40	39	38	37	...	31	...	27	26	25	24	23	22	21	...	15	...	11	10	9	8	7	6	...	0
RGB565	0	R4	...	R0								G5	...	G1	G0							B4	...	B0							
RGB666	1	R5	...	R1	R0							G5	...	G1	G0							B5	...	B1	B0						
RGB888	2	R7	...	R3	R2	R1	R0					G7	...	G3	G2	G1	G0					B7	...	B3	B2	B1	B0				
RGB101010	3	R9	...	R5	R4	R3	R2	R1	R0			G9	...	G5	G4	G3	G2	G1	G0			B9	...	B5	B4	B3	B2	B1	B0		

DC8200 has a DP and a DPI interface for each panel. And the YUV data mapping in the DP data is displayed in the following table. YUV422 CFG1 and YUV420 CFG3 formats support signal connection integration.

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Figure 5-4 DC8200 DP Data Mapping

| | | |

Figure 5-6 HDMI Data Mapping

Video Format	pin_ch2_r[11:0]	pin_ch1_g[11:0]	pin_ch0_b[11:0]
8-bit RGB	{R[7:0],4'b0}	{G[7:0],4'b0}	{B[7:0],4'b0}
10-bit RGB	{R[9:0],2'b0}	{G[9:0],2'b0}	{B[9:0],2'b0}
12-bit RGB	R[11:0]	G[11:0]	B[11:0]
8-bit YCbCr444	{Cr[7:0],4'b0}	{Y[7:0],4'b0}	{Cb[7:0],4'b0}
10-bit YCbCr444	{Cr[9:0],2'b0}	{Y[9:0],2'b0}	{Cb[9:0],2'b0}
12-bit YCbCr444	Cr [11:0]	Y [11:0]	Cb[11:0]
8-bit YCbCr422	12'b0	{Y(n)[7:0], 4'b0}/ {Y(n+1)[7:0], 4'b0}	{Cb(n)[7:0], 4'b0}/ {Cr(n)[7:0], 4'b0}/
10-bit YCbCr422	12'b0	{Y(n)[9:0], 2'b0}/ {Y(n+1)[9:0], 2'b0}	{Cb(n)[9:0], 2'b0}/ {Cr(n)[9:0], 2'b0}
12-bit YCbCr422	12'b0	Y(n)[11:0]/ Y(n+1)[11:0]	Cb(n)[11:0]/ Cr(n)[11:0]
8-bit YCbCr420	{Y(L)(n)[7:0],4'b0}	{Y(L)(n+1)[7:0],4'b0}	{Cb(L)(n)[7:0], 4'b0}
	{Y(L+1)(n)[7:0],4'b0}	{Y(L+1)(n+1)[7:0],4'b0}	{Cr (L+1)(n)[7:0], 4'b0}
10-bit YCbCr420	{Y(L)(n)[9:0],2'b0}	{Y(L)(n+1)[9:0],2'b0}	{Cb(L)(n)[9:0], 2'b0}
	{Y(L+1)(n)[9:0],2'b0}	{Y(L)(n+1)[9:0],2'b0}	{Cr(L+1)(n)[9:0], 2'b0}
12-bit YCbCr420	Y(L)(n) [11:0]	Y(L)(n+1) [11:0]	Cb(L)(n)[11:0]
	Y(L+1)(n) [11:0]	Y(L+1)(n+1) [11:0]	Cr (L+1)(n)[11:0]

5.6. Control Registers

5.6.1. DOM VOUT CRG

The Control Registers of **dom_vout_crg** are described in the following tables.

clk_apb

Table 5-5 clk_apb Register Description

Offset Address: 16'h0			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h4	Clock divider coefficient: • Max: 8 • Default: 4 • Min: 4 • Typical: 4

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clk_dc8200_pix0

Table 5-6 clk_dc8200_pix0 Register Description

Offset Address: 16'h4			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h4	Clock divider coefficient: • Max: 63 • Default: 4 • Min: 4 • Typical: 4

clk_dsi_sys

Table 5-7 clk_dsi_sys Register Description

Offset Address: 16'h8			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h4	Clock divider coefficient: • Max: 31 • Default: 4 • Min: 4 • Typical: 4

clk_tx_esc

Table 5-8 clk_tx_esc Register Description

Offset Address: 16'hc			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	Reserved	0	Reserved
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	clk_divcfg	24'h12	Clock divider coefficient:

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Table 5-8 clk_tx_esc Register Description (continued)

Offset Address: 16'hc			
Access: RW			
Bit	**Name**	**Default**	**Description**
			• Max: 31 • Default: 12 • Min: 10 • Typical: 12

clk_u0_dc8200_clk_axi

Table 5-9 clk_u0_dc8200_clk_axi Register Description

Offset Address: 16'h10			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_dc8200_clk_core

Table 5-10 clk_u0_dc8200_clk_core Register Description

Offset Address: 16'h14			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_dc8200_clk_ahb

Table 5-11 clk_u0_dc8200_clk_ahb Register Description

Offset Address: 16'h18			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: clock enable • 0: clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_dc8200_clk_pix0

Table 5-12 clk_u0_dc8200_clk_pix0 Register Description

Offset Address: 16'h1c			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6"h0	Clock multiplexing selector: • clk_dc8200_pix0 • clk_hdmitx0_pixelclk
[0:23]	Reserved	0	Reserved

clk_u0_dc8200_clk_pix1

Table 5-13 clk_u0_dc8200_clk_pix1 Register Description

Offset Address: 16'h20			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6"h0	Clock multiplexing selector: • clk_dc8200_pix0 • clk_hdmitx0_pixelclk

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Table 5-13 clk_u0_dc8200_clk_pix1 Register Description (continued)

Offset Address: 16'h20			
Access: RW			
Bit	**Name**	**Default**	**Description**
[0:23]	Reserved	0	Reserved

clk_dom_vout_top_lcd_clk

Table 5-14 clk_dom_vout_top_lcd_clk Register Description

Offset Address: 16'h24			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6"h0	Clock multiplexing selector: • u0_dc8200.clk_pix0_out • u0_dc8200.clk_pix1_out
[0:23]	Reserved	0	Reserved

clk_u0_cdns_dsiTx_clk_apb

Table 5-15 clk_u0_cdns_dsiTx_clk_apb Register Description

Offset Address: 16'h28			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_cdns_dsiTx_clk_sys

Table 5-16 clk_u0_cdns_dsiTx_clk_sys Register Description

Offset Address: 16'h2c			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_cdns_dsiTx_clk_dpi

Table 5-17 clk_u0_cdns_dsiTx_clk_dpi Register Description

Offset Address: 16"30			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	clk_mux_sel	6"h0	Clock multiplexing selector: • clk_dc8200_pix0 • clk_hdmitx0_pixelclk
[0:23]	Reserved	0	Reserved

clk_u0_cdns_dsiTx_clk_txesc

Table 5-18 clk_u0_cdns_dsiTx_clk_txesc Register Description

Offset Address: 16'h34			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_mipitx_dphy_clk_txesc

Table 5-19 clk_u0_cdns_dsiTx_clk_txesc Register Description

Offset Address: 16'h38			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_hdmi_tx_clk_mclk

Table 5-20 clk_u0_hdmi_tx_clk_mclk Register Description

Offset Address: 16'h3c			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

clk_u0_hdmi_tx_clk_bclk

Table 5-21 clk_u0_hdmi_tx_clk_bclk Register Description

Offset Address: 16'h40			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

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clk_u0_hdmi_tx_clk_sys

Table 5-22 clk_u0_hdmi_tx_clk_sys Register Description

Offset Address: 16'h44			
Access: RW			
Bit	**Name**	**Default**	**Description**
[31]	clk_icg	0	• 1: Clock enable • 0: Clock disable
[30]	Reserved	0	Reserved
[24:29]	Reserved	0	Reserved
[0:23]	Reserved	0	Reserved

Software_RESET_assert0_addr_assert_sel

Table 5-23 Software_RESET_assert0_addr_assert_sel Register Description

Offset Address: 16'h38			
Access: RW			
Bit	**Name**	**Default**	**Description**
[0]	rstn_u0_dc8200_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u0_dc8200_rstn_ahb	1	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_dc8200_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_cdns_dsiTx_rstn_dpi	1	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_cdns_dsiTx_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_cdns_dsiTx_rstn_rxesc	1	• 1: Assert reset • 0: De-assert reset
[6]	rstn_u0_cdns_dsiTx_rstn_sys	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u0_cdns_dsiTx_rstn_txbytehs	1	• 1: Assert reset • 0: De-assert reset

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Table 5-23 Software_RESET_assert0_addr_assert_sel Register Description (continued)

Offset Address: 16'h38			
Access: RW			
Bit	**Name**	**Default**	**Description**
[8]	rstn_u0_cdns_dsiTx_rstn_txesc	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_hdmi_tx_rstn_hdmi	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_mipitx_dphy_rstn_sys	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_mipitx_dphy_rstn_txbytehs	1	• 1: Assert reset • 0: De-assert reset
[31:12]	Reserved	0	Reserved

VOUTCRG_RESET_STATUS

Table 5-24 VOUTCRG_RESET_STATUS Register Description

Offset Address: 16'h4c			
Access: RW			
Bit	**Name**	**Default**	**Description**
[0]	rstn_u0_dc8200_rstn_axi	1	• 1: Assert reset • 0: De-assert reset
[1]	rstn_u0_dc8200_rstn_ahb	1	• 1: Assert reset • 0: De-assert reset
[2]	rstn_u0_dc8200_rstn_core	1	• 1: Assert reset • 0: De-assert reset
[3]	rstn_u0_cdns_dsiTx_rstn_dpi	1	• 1: Assert reset • 0: De-assert reset
[4]	rstn_u0_cdns_dsiTx_rstn_apb	1	• 1: Assert reset • 0: De-assert reset
[5]	rstn_u0_cdns_dsiTx_rstn_rxesc	1	• 1: Assert reset • 0: De-assert reset

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Table 5-24 VOUTCRG_RESET_STATUS Register Description (continued)

Offset Address: 16'h4c			
Access: RW			
Bit	**Name**	**Default**	**Description**
[6]	rstn_u0_cdns_dsiTx_rstn_sys	1	• 1: Assert reset • 0: De-assert reset
[7]	rstn_u0_cdns_dsiTx_rstn_txbytehs	1	• 1: Assert reset • 0: De-assert reset
[8]	rstn_u0_cdns_dsiTx_rstn_txesc	1	• 1: Assert reset • 0: De-assert reset
[9]	rstn_u0_hdmi_tx_rstn_hdmi	1	• 1: Assert reset • 0: De-assert reset
[10]	rstn_u0_mipitx_dphy_rstn_sys	1	• 1: Assert reset • 0: De-assert reset
[11]	rstn_u0_mipitx_dphy_rstn_txbytehs	1	• 1: Assert reset • 0: De-assert reset
[31:12]	Reserved	0	Reserved

5.6.2. DOM VOUT SYSCON

The Control Registers of **dom_vout_syscon** are described in the following tables.

DOM_VOUT_SYSCONSAIF__SYSCFG_0

Table 5-25 DOM_VOUT_SYSCONSAIF__SYSCFG_0 Register Description

Offset Address: 0x0				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[7:0]	u0_cdns_dsiTx_SCFG_sram_-config	WR	0x0	SRAM configuration: • [0]: SD, shut down enable, high active. • [1]: SLP, sleep enable, high active.
[23:8]	u0_cdns_dsiTx_dsi_test_-generic_ctrl	RO	0x0	
[31:24]	Reserved	None	0x0	Reserved

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DOM_VOUT_SYSCONSAIF__SYSCFG_4

Table 5-26 DOM_VOUT_SYSCONSAIF__SYSCFG_4 Register Description

Offset Address: 0x4				
Default: 0x80000				
Bit	**Name**	**Access**	**Default**	**Description**
[15:0]	u0_cdns_dsiTx_dsi_test_-generic_status	WR	0x0	
[16]	u0_dc8200_CACTIVE	RO	0x0	
[17]	u0_dc8200_CSYSACK	RO	0x0	
[18]	u0_dc8200_CSYSREQ	WR	0x0	
[19]	u0_dc8200_disableRamClock-Gating	WR	0x1	
[20]	u0_display_panel_mux_pan-el_sel	WR	0x0	DC8200 panel: • 0 - Panel 0 • 1 - Panel 1
[23:21]	u0_dsiTx_data_mapping_d-p_mode	WR	0x0	DP color mode: • 0 - YUV420 CFG1 • 1 - YUV420 CFG3 • 2 - YUV422 CFG1 (Reserved) • 3 - RGB888 • 4 - RGB101010/RGB666 • 5 - RGB565
[24]	u0_dsiTx_data_mapping_d-pi_dp_sel	WR	0x0	DC8200 DP/DPI interface for dsiTx: • 0 - DPI • 1 - DP
[25]	u0_hdmi_data_mapping_d-p_bit_depth	WR	0x0	DP bit depth: • 0 - 8 bit • 1 - 10 bit
[27:26]	u0_hdmi_data_mapping_d-p_yuv_mode	WR	0x0	DP YUV mode: • 0 - YUV420 • 1 - YUV422 • 2 - YUV444 • 3 - RGB
[29:28]	u0_hdmi_data_mapping_d-pi_bit_depth	WR	0x0	DPI bit depth:

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Table 5-26 DOM_VOUT_SYSCONSAIF__SYSCFG_4 Register Description (continued)

Offset Address: 0x4				
Default: 0x80000				
Bit	**Name**	**Access**	**Default**	**Description**
				• 0 - 8 bit • 1 - 10 bit • 2 - 6 bit CFG1 in DC8200 • 3 - RGB565 CFG1 in DC8200
[30]	u0_hdmi_data_mapping_dpi_dp_sel	WR	0x0	DC8200 DP/DPI interface: • 0 - DPI • 1 - DP
[31]	Reserved	None	0x0	Reserved

DOM_VOUT_SYSCONSAIF__SYSCFG_8

Table 5-27 DOM_VOUT_SYSCONSAIF__SYSCFG_8 Register Description

Offset Address: 0x8				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[1:0]	u0_lcd_data_mapping_dp_rgb_fmt	WR	0x0	RGB format in DP data: • 0 - RGB888 • 1 - RGB666 • 2 - RGB565
[2]	u0_lcd_data_mapping_dpi_dp_sel	WR	0x0	DPI or DP: • 0 - DPI • 1 - DP
[3]	u1_display_panel_mux_panel_sel	WR	0x0	DC8200 panel: • 0 - Panel 0 • 1 - Panel 1
[4]	u2_display_panel_mux_panel_sel	WR	0x0	DC8200 panel: • 0 - Panel 0 • 1 - Panel 1
[31:5]	Reserved	None	0x0	Reserved

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DOM_VOUT_SYSCONSAIF__SYSCFG_12

Table 5-28 DOM_VOUT_SYSCONSAIF__SYSCFG_12 Register Description

Offset Address: 0xc				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	vout_test_reg0	WR	0x0	

DOM_VOUT_SYSCONSAIF__SYSCFG_16

Table 5-29 DOM_VOUT_SYSCONSAIF__SYSCFG_16 Register Description

Offset Address: 0x10				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	vout_test_reg1	WR	0x0	

DOM_VOUT_SYSCONSAIF__SYSCFG_20

Table 5-30 DOM_VOUT_SYSCONSAIF__SYSCFG_20 Register Description

Offset Address: 0x14				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	vout_test_reg2	WR	0x0	

DOM_VOUT_SYSCONSAIF__SYSCFG_24

Table 5-31 DOM_VOUT_SYSCONSAIF__SYSCFG_24 Register Description

Offset Address: 0x18				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	vout_test_reg3	WR	0x0	

5.6.3. MIPITX APBIF

The Control Registers of **mipitx_apbif** are described in the following tables.

MIPITX_APBIFSAIF__SYSCFG_0

Table 5-32 MIPITX_APBIFSAIF__SYSCFG_0 Register Description

Offset Address: 0x0				
Default: 0x111a021				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	u0_mipitx_dphy_AON_POWER_READY_N	WR	0x1	

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Table 5-32 MIPITX_APBIFSAIF__SYSCFG_0 Register Description (continued)

Offset Address: 0x0				
Default: 0x111a021				
Bit	**Name**	**Access**	**Default**	**Description**
[5:1]	u0_mipitx_dphy_CFG_CKLANE_SET	WR	0x10	
[6]	u0_mipitx_dphy_CFG_DATABUS16_SEL	WR	0x0	
[11:7]	u0_mipitx_dphy_CFG_DPDN_SWAP	WR	0x0	
[14:12]	u0_mipitx_dphy_CFG_L0_SWAP_SEL	WR	0x2	
[17:15]	u0_mipitx_dphy_CFG_L1_SWAP_SEL	WR	0x3	
[20:18]	u0_mipitx_dphy_CFG_L2_SWAP_SEL	WR	0x4	
[23:21]	u0_mipitx_dphy_CFG_L3_SWAP_SEL	WR	0x0	
[26:24]	u0_mipitx_dphy_CFG_L4_SWAP_SEL	WR	0x1	
[31:27]	Reserved	None	0x0	Reserved

MIPITX_APBIFSAIF__SYSCFG_4

Table 5-33 MIPITX_APBIFSAIF__SYSCFG_4 Register Description

Offset Address: 0x4				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_MPOSV_31_0_	RO	0x0	

MIPITX_APBIFSAIF__SYSCFG_8

Table 5-34 MIPITX_APBIFSAIF__SYSCFG_8 Register Description

Offset Address: 0x8				
Default: 0x10800000				
Bit	**Name**	**Access**	**Default**	**Description**
[14:0]	u0_mipitx_dphy_MPOSV_46_32_	RO	0x0	
[15]	u0_mipitx_dphy_RGS_CDTX_PLL_FM_CPLT	RO	0x0	
[16]	u0_mipitx_dphy_RGS_CDTX_PLL_FM_OVER	RO	0x0	
[17]	u0_mipitx_dphy_RGS_CDTX_PLL_FM_UNDER	RO	0x0	
[18]	u0_mipitx_dphy_RGS_CDTX_PLL_UNLOCK	RO	0x0	
[23:19]	u0_mipitx_dphy_RG_CDTX_L0N_HSTX_RES	WR	0x10	
[28:24]	u0_mipitx_dphy_RG_CDTX_L0P_HSTX_RES	WR	0x10	
[31:29]	Reserved	None	0x0	Reserved

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MIPITX_APBIFSAIF__SYSCFG_12

Table 5-35 MIPITX_APBIFSAIF__SYSCFG_12 Register Description

Offset Address: 0xc				
Default: 0x21084210				
Bit	**Name**	**Access**	**Default**	**Description**
[4:0]	u0_mipitx_dphy_RG_CDTX_L1N_HSTX_RES	WR	0x10	
[9:5]	u0_mipitx_dphy_RG_CDTX_L1P_HSTX_RES	WR	0x10	
[14:10]	u0_mipitx_dphy_RG_CDTX_L2N_HSTX_RES	WR	0x10	
[19:15]	u0_mipitx_dphy_RG_CDTX_L2P_HSTX_RES	WR	0x10	
[24:20]	u0_mipitx_dphy_RG_CDTX_L3N_HSTX_RES	WR	0x10	
[29:25]	u0_mipitx_dphy_RG_CDTX_L3P_HSTX_RES	WR	0x10	
[30:31]	Reserved	None	0x0	Reserved

MIPITX_APBIFSAIF__SYSCFG_16

Table 5-36 MIPITX_APBIFSAIF__SYSCFG_16 Register Description

Offset Address: 0x10				
Default: 0x210				
Bit	**Name**	**Access**	**Default**	**Description**
[4:0]	u0_mipitx_dphy_RG_CDTX_L4N_HSTX_RES	WR	0x10	
[9:5]	u0_mipitx_dphy_RG_CDTX_L4P_HSTX_RES	WR	0x10	
[10:31]	Reserved	None	0x0	Reserved

MIPITX_APBIFSAIF__SYSCFG_20

Table 5-37 MIPITX_APBIFSAIF__SYSCFG_20 Register Description

Offset Address: 0x14				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:23]	u0_mipitx_dphy_RG_CDTX_PLL_FBK_FRA	WR	0x0	
[31:24]	Reserved	None	0x0	Reserved

MIPITX_APBIFSAIF__SYSCFG_24

Table 5-38 MIPITX_APBIFSAIF__SYSCFG_24 Register Description

Offset Address: 0x18				
Default: 0x864				
Bit	**Name**	**Access**	**Default**	**Description**
[8:0]	u0_mipitx_dphy_RG_CDTX_PLL_FBK_INT	WR	0x64	
[9]	u0_mipitx_dphy_RG_CDTX_PLL_FM_EN	WR	0x0	

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Table 5-38 MIPITX_APBIFSAIF__SYSCFG_24 Register Description (continued)

Offset Address: 0x18				
Default: 0x864				
Bit	**Name**	**Access**	**Default**	**Description**
[10]	u0_mipitx_dphy_RG_CDTX_PLL_LDO_STB_X2_EN	WR	0x0	
[12:11]	u0_mipitx_dphy_RG_CDTX_PLL_PRE_DIV	WR	0x1	
[30:13]	u0_mipitx_dphy_RG_CDTX_PLL_SSC_DELTA	WR	0x0	
[31]	Reserved	None	0x0	Reserved

MIPITX_APBIFSAIF__SYSCFG_28

Table 5-39 MIPITX_APBIFSAIF__SYSCFG_28 Register Description

Offset Address: 0x1c				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[17:0]	u0_mipitx_dphy_RG_CDTX_PLL_SSC_DELTA_INIT	WR	0x0	
[18]	u0_mipitx_dphy_RG_CDTX_PLL_SSC_EN	WR	0x0	
[28:19]	u0_mipitx_dphy_RG_CDTX_PLL_SSC_PRD	WR	0x0	
[31:29]	Reserved	None	0x0	Reserved

MIPITX_APBIFSAIF__SYSCFG_32

Table 5-40 MIPITX_APBIFSAIF__SYSCFG_32 Register Description

Offset Address: 0x20				
Default: 0x530b0000				
Bit	**Name**	**Access**	**Default**	**Description**
[7:0]	u0_mipitx_dphy_RG_CLANE_HS_CLK_POST_TIME	WR	0x0	
[15:8]	u0_mipitx_dphy_RG_CLANE_HS_CLK_PRE_TIME	WR	0x0	
[23:16]	u0_mipitx_dphy_RG_CLANE_HS_PRE_TIME	WR	0xb	
[31:24]	u0_mipitx_dphy_RG_CLANE_HS_TRAIL_TIME	WR	0x53	

MIPITX_APBIFSAIF__SYSCFG_36

Table 5-41 MIPITX_APBIFSAIF__SYSCFG_36 Register Description

Offset Address: 0x24				
Default: 0x21160e16				
Bit	**Name**	**Access**	**Default**	**Description**
[7:0]	u0_mipitx_dphy_RG_CLANE_HS_ZERO_TIME	WR	0x16	
[15:8]	u0_mipitx_dphy_RG_DLANE_HS_PRE_TIME	WR	0xe	
[23:16]	u0_mipitx_dphy_RG_DLANE_HS_TRAIL_TIME	WR	0x16	

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Table 5-41 MIPITX_APBIFSAIF__SYSCFG_36 Register Description (continued)

Offset Address: 0x24				
Default: 0x21160e16				
Bit	**Name**	**Access**	**Default**	**Description**
[31:24]	u0_mipitx_dphy_RG_DLANE_HS_ZERO_TIME	WR	0x21	

MIPITX_APBIFSAIF__SYSCFG_40

Table 5-42 MIPITX_APBIFSAIF__SYSCFG_40 Register Description

Offset Address: 0x28				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[2:0]	u0_mipitx_dphy_RG_EXTD_CYCLE_SEL	WR	0x0	
[31:3]	Reserved	None	0x0	Reserved

MIPITX_APBIFSAIF__SYSCFG_44

Table 5-43 MIPITX_APBIFSAIF__SYSCFG_44 Register Description

Offset Address: 0x2c				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
31:0]	u0_mipitx_dphy_SCFG_c_hs_pre_zero_time	WR	0x0	

MIPITX_APBIFSAIF__SYSCFG_48

Table 5-44 MIPITX_APBIFSAIF__SYSCFG_48 Register Description

Offset Address: 0x30				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0]	u0_mipitx_dphy_SCFG_dphy_src_sel	WR	0x0	
[1:2]	u0_mipitx_dphy_SCFG_dsi_txready_esc_sel	WR	0x0	
[4:3]	u0_mipitx_dphy_SCFG_ppi_c_ready_sel	WR	0x0	
[9:5]	u0_mipitx_dphy_VCONTROL	WR	0x0	
[10:31]	Reserved	None	0x0	Reserved

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MIPITX_APBIFSAIF__SYSCFG_52

Table 5-45 MIPITX_APBIFSAIF__SYSCFG_52 Register Description

Offset Address: 0x34				
Default: 0x87654321				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW00	WR	0x87654321	

MIPITX_APBIFSAIF__SYSCFG_56

Table 5-46 MIPITX_APBIFSAIF__SYSCFG_56 Register Description

Offset Address: 0x38				
Default: 0xfedcba9				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW01	WR	0xfedcba9	

MIPITX_APBIFSAIF__SYSCFG_60

Table 5-47 MIPITX_APBIFSAIF__SYSCFG_60 Register Description

Offset Address: 0x3c				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW02	WR	0x0	

MIPITX_APBIFSAIF__SYSCFG_64

Table 5-48 MIPITX_APBIFSAIF__SYSCFG_64 Register Description

Offset Address: 0x40				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW03	WR	0x0	

MIPITX_APBIFSAIF__SYSCFG_68

Table 5-49 MIPITX_APBIFSAIF__SYSCFG_68 Register Description

Offset Address: 0x44				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW04	WR	0x0	

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MIPITX_APBIFSAIF__SYSCFG_72

Table 5-50 MIPITX_APBIFSAIF__SYSCFG_72 Register Description

Offset Address: 0x48				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW05	WR	0x0	

MIPITX_APBIFSAIF__SYSCFG_76

Table 5-51 MIPITX_APBIFSAIF__SYSCFG_76 Register Description

Offset Address: 0x4c				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW06	WR	0x0	

MIPITX_APBIFSAIF__SYSCFG_80

Table 5-52 MIPITX_APBIFSAIF__SYSCFG_80 Register Description

Offset Address: 0x50				
Default: 0x21084210				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW07	WR	0x21084210	

MIPITX_APBIFSAIF__SYSCFG_84

Table 5-53 MIPITX_APBIFSAIF__SYSCFG_84 Register Description

Offset Address: 0x54				
Default: 0x84210				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW08	WR	0x84210	

MIPITX_APBIFSAIF__SYSCFG_88

Table 5-54 MIPITX_APBIFSAIF__SYSCFG_88 Register Description

Offset Address: 0x58				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW09	WR	0x0	

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MIPITX_APBIFSAIF__SYSCFG_92

Table 5-55 MIPITX_APBIFSAIF__SYSCFG_92 Register Description

Offset Address: 0x5c				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW0A	WR	0x0	

MIPITX_APBIFSAIF__SYSCFG_96

Table 5-56 MIPITX_APBIFSAIF__SYSCFG_96 Register Description

Offset Address: 0x60				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[0:31]	u0_mipitx_dphy_XCFGI_DW0B	WR	0x0	

MIPITX_APBIFSAIF__SYSCFG_100

Table 5-57 MIPITX_APBIFSAIF__SYSCFG_100 Register Description

Offset Address: 0x64				
Default: 0x0				
Bit	**Name**	**Access**	**Default**	**Description**
[7:0]	u0_mipitx_dphy_dbg1_mux_dout	RO	0x0	
[12:8]	u0_mipitx_dphy_dbg1_mux_sel	WR	0x0	
[20:13]	u0_mipitx_dphy_dbg2_mux_dout	RO	0x0	
[25:21]	u0_mipitx_dphy_dbg2_mux_sel	WR	0x0	
[28:26]	u0_mipitx_dphy_refclk_in_sel	WR	0x0	
[29]	u0_mipitx_dphy_resetb	WR	0x0	
[30:31]	Reserved	None	0x0	Reserved

5.7. More Information

DC8200

If you still need more information on the DC8200 of JH-7110, contact StarFive and request the following documentation.

- DC8200 control register list reference: *DC8200 Dual Display Controller DPU IP Exposed Accessible Registers (STF Edition)*
- DC8200 control register feature reference: *DC8200 Dual Display Controller IP Hardware Features (STF Edition)*

cdns_dsiTx

If you still need more information on the cdns_dsiTx of JH-7110, contact StarFive and request the following documentation.

- *MIPI DSI v1.3.1 Host Controller User Guide*

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HDMI

If you still need more information on the HDMI of JH-7110, contact StarFive and request the following documentation.

- *INNO HDMI2.0 TRANSMITTER For TSMC28HPC+ Datasheet*

MIPITX DPHY

If you still need more information on the MIPITX DPHY of JH-7110, contact StarFive and request the following documentation.

- *M31DPHYTX512TL028D MIPI D-PHY Transmitter of TSMC 28nm Logic 0.9/1.8V High Performance Compact Plus Process*

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6. Glossary

6.1. AON

Always-On.

6.2. DRAM

Dynamic Random Access Memory.

6.3. eDRAM

Embedded DRAM.

6.4. Instruction Set

A group of commands for a CPU in machine language that can refer to all possible instructions for a CPU, or a subset of instructions to enhance its performance in specific situations, and includes:

- Instruction length - which can vary, Opcodes - the command to be carried out.
- Operands - on which the command will operate.
- Registers - internal locations that are limited in number and ability while quick to access.
- Memory - external storage - a larger and more versatile number of locations that are slower to access.

6.5. ISA

Instruction Set Architecture.

6.6. Latch

A circuit that has two stable states that is used to store state information, known as a bi-stable multi-vibrator.

6.7. LPDDR

Low Power Double Data Rate

6.8. MIPS

Microprocessor without Interlocked Pipelined Stages—a *reduced instruction set computer (RISC)* instruction set architecture developed by MIPS Computer Systems, now MIPS Technologies, based in the United States, that influenced later RISC architectures.

6.9. MMU

Memory Management Unit.

6.10. MODE

A field within an instruction or instruction set that specifies the way the operand or the effective address is determined.

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6.11. MSI

Message Signal Interrupt.

6.12. OS-level Sandboxing

A form of sandboxing implemented by the pointer masking proposal. There is no guarantee that sandboxed code cannot modify the pointer mask and therefore the sandbox does not allow modifying pointer masks in user mode.

6.13. PD

Short for pull down. When talking about PD in circuit layout, it is always used to indicate the need of a pull-down resistor (PD).

Pull-up and Pull-down resistors are used to correctly bias the inputs of digital gates to stop them from floating about randomly when there is no input condition

6.14. PLIC

Platform-Level Interrupt Controller. The PLIC is a device designed to handle interrupts other than timer and software in RISC-V.

6.15. Privileged

Provides security isolation, and a means to reduce code defects because code does not have to check for illegal values. Privileged contains state, is used primarily to run applications and can be used to debug implementations. It defines CSR address space and content trap when taken increases privilege mode (say from U to S) trap when taken stays at the current privilege mode access more than even M mode. Its addresses reserved in ISA. address includes highest mode that access the CSR and if it is `r/w/rw/none` preserve bits already there when you change a field.

6.16. Profile

ISA Profile is a set of extensions (instructions, state and behaviors) that users can depend on working together. Extensions are either required, optional, unsupported, or incompatible. RISC-V has defined two Profile types: Application (RVAyy)--appropriate for Linux-class and other embedded designs with more sophisticated ISA needs—and Micro-controller (RVMyy)-- appropriate for cost-sensitive application-optimized embedded designs running bare-metal or simple RTOS environments.

6.17. Pseudo Instructions

In support of a core design goal for RISC-V ISA - high-performance - pseudo instructions often include special commands to the assembler. The use of pseudo instructions supports a policy of keeping the instruction set as small as possible, while supporting optimization and adding clarity to software programming. For example, the use of a pseudo instruction enables loading into memory with a 32-bit offset (called big) that is not directly available, because only 16-bit offsets are permitted.

6.18. PTE

Page Table Entry - an entry in the data structure used by a virtual memory system in a computer operating system to store the mapping between virtual addresses (used by the program executed by the accessing process) and physical addresses (used by the hardware, or more specifically, by the RAM subsystem), that enables access data in memory

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6.19. PU

Short for pull up. When talking about PU in circuit layout, it is always used to indicate the need of a pull-up resistor (PU).

Pull-up and Pull-down resistors are used to correctly bias the inputs of digital gates to stop them from floating about randomly when there is no input condition

6.20. PTEP

Parallel Telemetry Processor - a high- speed virtual processor architecture.

6.21. Register

A group of flip-flops with each flip-flop capable of storing one bit of information. The simplest register is one that consists of only flip-flops with no external gates.

6.22. RISC

Reduced Instruction Set Computer architecture. Information processing using any of a family of microprocessors that are designed to execute computing tasks with the simplest instructions in the shortest amount of time possible. RISC-based machines execute one instruction per clock cycle as opposed to CISC (Complex Instruction Set Computer) machines that can have special instructions as well as instructions that take more than one cycle to execute.

6.23. Segmentation fault

A failure condition caused by a memory access violation in hardware operating with memory protection. The fault process notifies the *operating system (OS)* that software has attempted to access a restricted area of memory.

6.24. SHA

Secure Hash Algorithms—a family of cryptographic hash functions published by the National Institute of Standards and Technology as a U.S. Federal Information Processing Standard that started with what is now known as SHA-0, a retronym used for the original (1993) 160-bit hash function published under the name "SHA".

6.25. SoC

System-on-a-Chip.

6.26. SRAM

Static Random Access Memory.

6.27. TRNG

True Random Number Generator - also known as HRNG, or Hardware Random Number Generator - a device that generates random numbers from a physical process, rather than by means of an algorithm. Such devices are often based on microscopic phenomena that generate low-level, statistically random "noise" signals, like thermal noise, the photoelectric effect involving a beam splitter, and other quantum phenomena.

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